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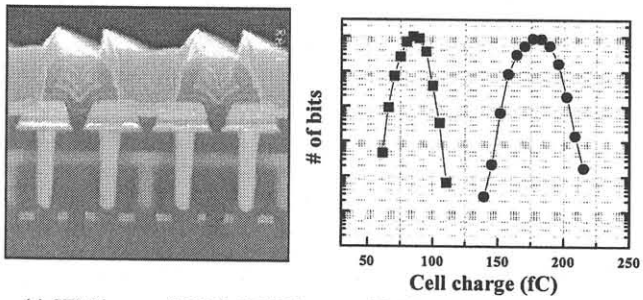
Highly Stable Etch Stopper Technology for 0.25 μm 1T1C 32Mb FRAM

N. W. Jang, Y. J. Song, S. H. Joo, K. M. Lee, H. H. Kim, H. J. Joo, J. H. Park, S. W. Lee, S. Y. Lee, and Kinam Kim

Advanced Technology Development Team, R&D Center, Memory Devices, Samsung Electronics Co. Ltd.,
San #24, Nongseo-Li, Kiheung-Eup, Yongin-Si, Kyungki-Do, Korea
Phone:+82-31-209-4970 Fax:+82-31-209-3274 E-mail:nwjang@samsung.co.kr

1. Introduction

32Mb FRAM device was recently developed using ultra thin 400nm capacitor stack, a noble metal etch stopper, and novel common cell-via scheme as shown in Figure 1 [1]. Unfortunately, there are still numerous integration challenges to overcome for producing commercial high-density FRAM devices. In particular, a wide sensing window is very critical factor for the commercial application. Figure 1 shows the charge distribution of 32Mb FRAM in which the sensing window of charge difference between data "1" and data "0" is very narrow. Since the narrow sensing window is not able to guarantee a reliable high yield at retention test, it is strongly desired to improve the sensing widow.



(a) SEM image of 32Mb FRAM (b) Charge distribution

Figure 1. SEM image and Charge distribution of 32Mb FRAM

By systematically investigating the narrow sensing window, it was found that the effective cell area of ferroelectric capacitor, which is closely related to the cell charge, substantially reduced during bottom electrode etching process. It is mainly due to the difficulty in etching noble electrode metals such as Ir and Pt [2]. Hence, in a given etching slope, in order to increase the effective cell area, the bottom electrode stack height should be reduced as low as possible. However, since the bottom electrode stack height is strongly correlated with buried contact (BC) resistance, it is prerequisite to enhance diffusion barrier properties of reduced bottom electrode stack. In this experiment, we propose a TiAlN oxygen stopping layer for enhancing the diffusion barrier layer, which makes it possible to reduce the bottom stack height from 180 nm to 90 nm, increasing the effective cell area by 20%. In addition, it is also very important to integrate the ultra thin capacitor stack without process degradation. As capacitor size and stack height scale down further, stress effect plays most vital role in degrading the ferroelectric capacitors during the integration process. Therefore, we developed a stable PE-SiN etch stopper for replacing noble metal etch stopper such as Ir and IrO2 that has strong stress variation and eventually deteriorates the cell charge distribution.

In this paper, we developed highly manufacturable 1T1C 32MFRAM by strong TiAlN oxygen stopping layer and novel PE-SiN etch stopper technology, which generates the wide sensing window, and thus guarantees a reliable high yield.

2. Experimental Technique

The CMOS transistors are fabricated by conventional processes such as STI isolation, retrograded twin well, poly-Si landing pad, and W-plug. A 300nm thick TiAlN oxidation barrier layer is deposited on this CMOS-processed substrate. Then, 50nm thick Pt, 20nm thick IrO_2, and 20nm thick Ir are sequentially deposited on TiAlN layer for bottom electrode stack. Sol-gel derived PTO films were prepared on bottom electrode as a seeding layer, and then 100nm thick PZT films were spin-coated on the as-deposited PTO films by using sol-gel technique. The PZT/PTO films were annealed at a low temperature of 600 °C for 1 min in O_2 atmosphere. Top electrode 50nm thick IrO_2 films and 70nm thick Ir electrode was sputter-deposited on the polycrystalline PZT films. After the ferroelectric capacitor formation, the whole capacitor stack was etched by using one photo mask. After patterning the ferroelectric capacitor stack, USG and SOG oxides were deposited on the patterned capacitor as interlayer dielectrics (ILD). The deposited ILD oxides were then etched back for planarization, which was followed by preparing PE-SiN layer as etch stopper in common cell via process. After the deposition of PE-SiN etching stopping layer, PSG was deposited as intermetallic dielectrics (IMD). Then, common cell via are defined on the top electrode. After final recovery annealing process, TiN/Al/TiN metal-2 for plate line was deposited and patterned.

3. Results.

Figure 2 illustrates the ferroelectric capacitor properties of 180nm and 90nm thick bottom electrode capacitors. The 90nm thick bottom stack capacitor shows higher polarization value and lower depolarization value than 180nm stack capacitor, because the effective cell area of 90nm BE stack capacitor is increased by 20%, and etch damage induced from BE etching process is reduced.

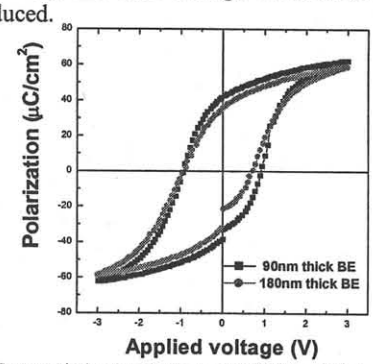


Figure 2. Hysteresis loops of 90nm and 180nm BE stack capacitors

Since the thickness of diffusion barrier layers was drastically reduced, it is necessary to evaluate the variation of buried contact (BC) resistance. It was observed that the contact resistance was maintained below 200Ω, indicating the strong oxygen barrier properties of diffusion barrier layers as shown in Figure 3.

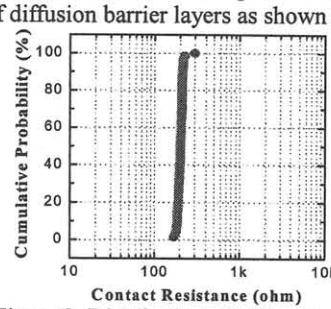


Figure 3. Distribution of BC contact resistance

It is also very important to maintain the ferroelectric properties without process degradation. It was found that the severe charge degradation occurred during the noble metal stopper process. Even though the charge values are degraded during the noble metal etch stopper process, it is not clearly determined whether the charge degradation originates from hydrogen damages, stress effects, or deposition temperature effects during noble metal etch stopper process. Therefore, a major source of charge degradation was investigated by changing the integrating process. Figure 4 shows the variations of polarization values as a function of process.

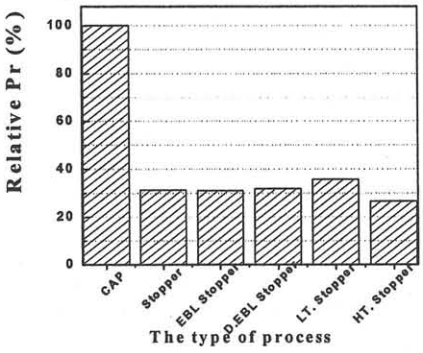
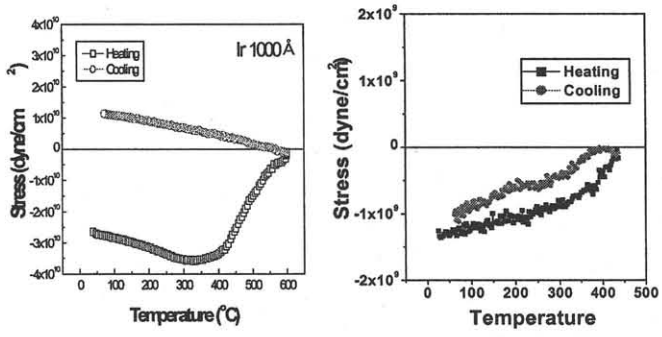


Figure 4. The variations of polarization values as a function of process

Figure 4 shows that the polarization value is severely decreased after depositing Ir film regardless of existing hydrogen blocking layer and deposition temperature. It implies that the stress of Ir film plays a dominant role in degrading the cell charge value. As the Ir noble metal is used as etch-stopper as well as bottom and top electrodes in 32MFRAM capacitors, the substrate shows severe stress variation from compressive to tensile during heating and cooling cycles due to the strong stress variation of Ir films, resulting in degrading the ferroelectric properties during integration as shown in Figure 5. Hence, it is desired to determine a proper etch stopper film, which should possess compressive stress and high etching selectivity against PSG film. Among several candidates, we select a PE-SiN film as the etch stopper layer due to its excellent etching selectivity against PSG oxide and highly stable compressive stress with low deposition temperature of 400 °C as shown in Figure 5.



(a) Ir film (b) PE-SiN film

Figure 5. The variations of stress a function of temperature.

Figure 6 illustrates fully processed 32Mb FRAM using ultra thin 90 nm BE capacitor stack and PE-SiN film as etch stopper. The ferroelectric capacitor using the PE-SiN stopper was successfully integrated into 32MFRAM without any processing issues. Figure 7 shows the variations of polarization values as a function of back-end process step for 32Mb FRAM devices. The cell charge value is not appreciable decreased after etch-stopper process, which implies that the PE-SiN films do not degrade the ferroelectric capacitor.

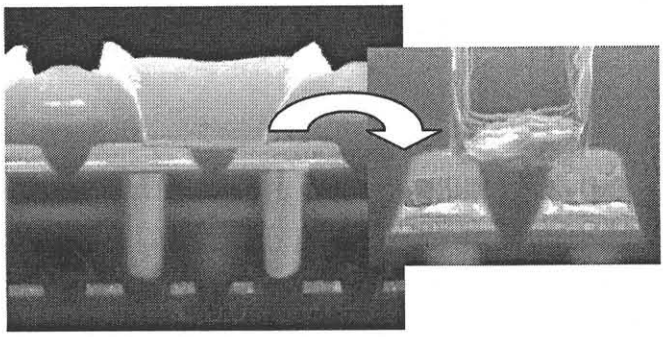


Figure 6. SEM image of fully processed 32Mb FRAM

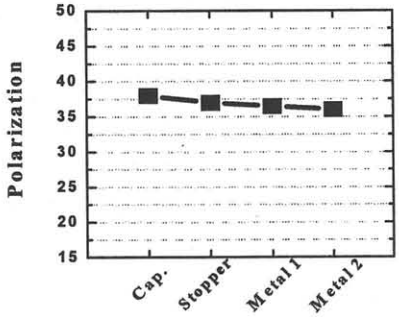


Figure 7. The variations of polarization values as a function of back-end process step

The measured charge distributions of data "1" and data "0" in 32Mb FRAM are shown in Figure 8, which illustrates very sharp and narrow charge distribution without tailing. This sharp charge distribution results in a wide sensing window, ***Qref = 100 fC*** for data "1" and data "0", which guarantees a reliable high yield.

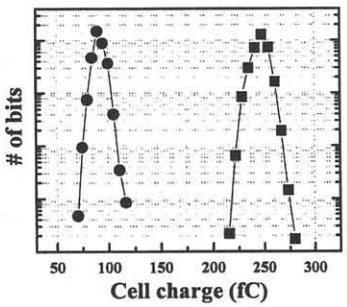


Figure 8. The measured charge distribution of 32Mb FRAM

4. Summary

In this paper, highly stable 0.25 μm 32Mb FRAM was developed using novel integration technologies such as ultra thin bottom electrode stack technology and PE-SiN etch stopper technology. The 32M FRAM device shows very wide sensing window, which guarantees a reliable high yield. Therefore, the novel integration technology strongly promises to provide a great possibility for high density FRAM to be used as stand-alone memory application.

References

[1] H. H. Kim, Y. J. Song, S. Y. Lee, H. J. Joo, N. W. Jang, D. J. Jung, Y. S. Park, S. O. Park,K. M. Lee, S. H. Joo, S. W. Lee, S. D. Nam, and Kinam Kim, VLSI Tech. Symp., (2002) (to appear).

[2] Y. J. Song, N. W. Jang, D. J. Jung, H. H. Kim, H. J. Joo, S. Y. Lee, K. M. Lee, S. H. Joo, S. O. Park, Kinam Kim, SSDM Symp., (2001) p.522