Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 84-85

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New multi layer top electrode of SRO/IrOx for 0.35μm FRAM

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1. Introduction

Smart cards or multi-purpose IC cards and highly secured electronic devices need high performance nonvolatile memory in the future. In these application, FRAM is the most suitable memory because of its high access speed and low power consumption. We reported that our 0.35 μm 256 kbit FRAM showed good performance [1], such as less than 50 ns access time at a low voltage of 3.3 V and good retention. It is also reported that $SrRuO_3$ (SRO) electrode improves ferroelectric properties [2,3]. We developed a new SRO/IrO_x top electrode system for FRAM. In this paper, we describe capacitors with our new developed SRO/IrO_x top electrode and its electric properties including hydrogen (H_2) endurance examination.

2. Device fabrication and characterization

Our newly developed ferroelectric capacitor consisted of SRO/IrO_x/PZT/Pt. This structure varies from previous bi-layer top electrodes [2] because the SRO film was not in direct contact with PZT. Figure 1 shows the cross sectional SEM image of 0.35 μm FRAM structure. PZT was deposited on Pt bottom electrode by sputtering method and crystallized by rapid thermal annealing. Multi-layer top electrode (TE) of SRO/IrO_x was deposited by sputtering. The conventional capacitor structure is almost the same as the new capacitor except for single IrO_x TE. The thickness of new SRO/IrO_x TE and conventional IrO_2 TE are about 200 nm. Patterned capacitors were encapsulated with a dielectric layer (encapsulation layer) eliminating hydrogen (H_2) diffusion into the capacitor. H_2 generated during metal or interlayer dielectric deposition is known to degrade the ferroelectric capacitor performance [3]. After capacitor fabrication, we adopted conventional triple Al layer interconnection and inter layer dielectric (ILD) process. Technology features are summarized in Table I.

The ferroelectric capacitor with our new SRO/IrOx multi TE shows superior performance to the conventional IrO_2 TE capacitor (Fig. 2). Switchable charge (Qsw) of 33 μC/cm^2 at 3 V operation was obtained on the new capacitors, while a Qsw of conventional capacitor was 23 μC/cm^2. In addition better lower voltage performance is obtained the with SRO/IrO_x multi layer TE. It indicates that the ferroelectric property is improved by the SRO.

Next, we investigated the H_2 endurance of ferroelectric capacitor to examine the capacitor degradation during Al interconnection and dielectric interlayer deposition. While capacitors with IrO_x TE degraded immediately, capacitors with SRO/IrO_x TE showed good H_2 endurance (Fig. 3). Changes in IrO_x TE surface from black to metallic indicate that IrO_x is reduced by H_2 and changes to metal rich IrO_x[3]. It is proposed that H_2 diffusion and reduction of the IrOx is slower with the SRO than that of the independent IrO_x TE. In other words, SRO acts a barrier or "H_2 blocker" to prevent the reduction of the IrO_x.

78 chips of 256 kbit FRAM are fabricated with our new capacitor. They show excellent retention (Fig. 4). No bit fail is observed until 504 hours at 150°C. It corresponds to more than 5 years reliability.

3. Conclusion

We developed SRO/IrO_x multi layered top electrode. Capacitors with the new top electrode have high initial switchable charge, and hydrogen degradation endurance. It indicates that the SRO top layer serves not only as an electrode but also as a H_2 blocker. 256 kbit FRAM with new capacitor showed excellent retention over 504 hours in 150°C.

References

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Table I. Technology feature of 0.35 μm FRAM

Gate length	0.35 μm
Ferro capacitor structure	SRO/IrOx/PZT/Pt
Source/Drain	TiSix
Via	W-plug
Metal	Triple Aluminum
Metal pitch	1.1 mm
Source voltage	3.0 V
Cell size	13.95 μm^2 (2T/2C) 8.69 μm^2 (1T1C)
Capacitor size	1.50 μm^2

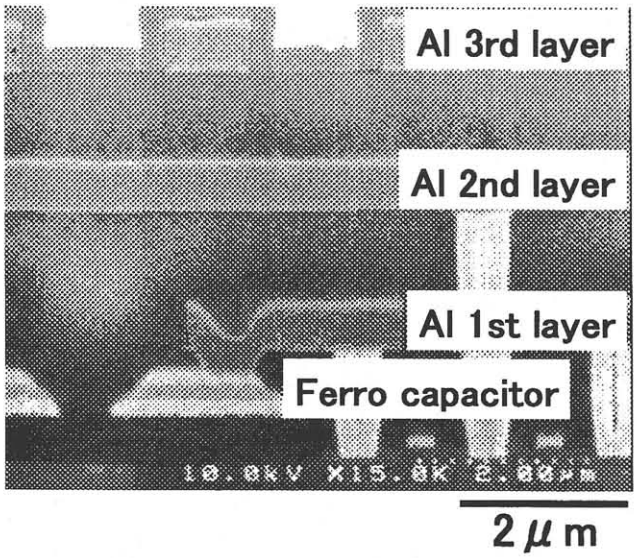

Fig. 1 Cross sectional view of 0.35 μm FRAM; Ferro capacitor is consited of SRO/IROx/PZT/Pt. Ferroelectrc capacitor is fabricated after conventional CMOS process.

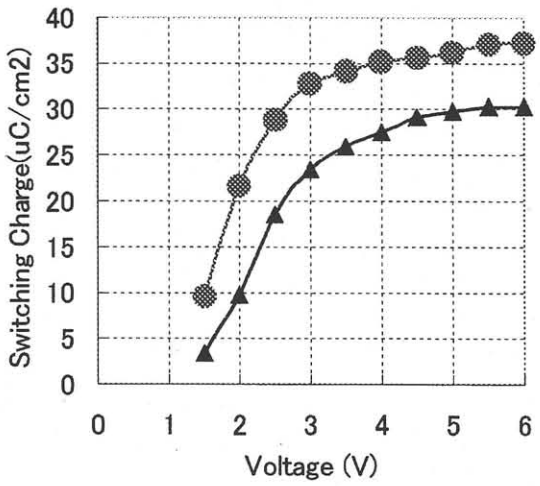

Fig.2 Comparison of Qtv between SRO/IrOx/PZT/Pt ferroelectric capacitor (circles) and IrO2/PZT/Pt ferroelectric capacitor (triangles). (50μm X 50μm capacitor)

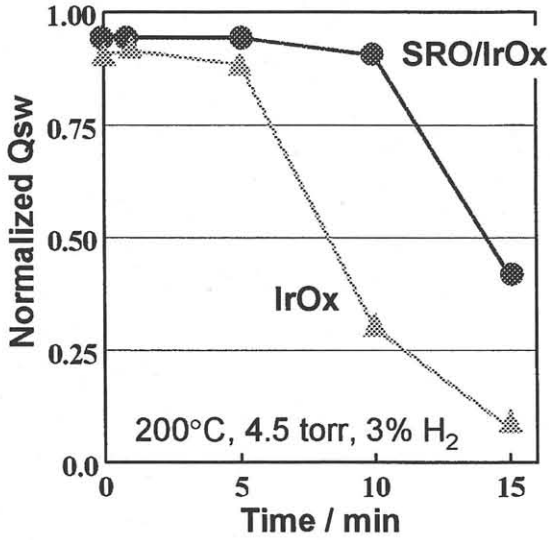

Fig. 3 Changes in switchable charge of capacitors with new SRO/IrOx top electrode (circles) and IrOx top electrode (triangles) during annealing in hydrogen atmosphere (200°C, 4.5torr, 3%)

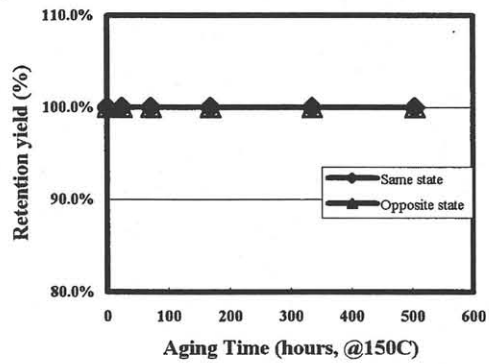

Fig. 4. 256 kbit FRAM retention performance with new SRO/IrOx multi layer TE capacitor; No bit fail appears even after 504 hours at 150°C.