D-4.1

Design of a Tiny Microprocessor
Based on the Single-Flux-Quantum Circuit Technology

N. Yoshikawa, F. Matsuzaki, N. Nakajima, K. Fujiwara, K. Yoda and K. Kawasaki

Yokohama National University, Graduate School of Engineering
79-5 Tokiwadai, Hodogaya-ku, Yokohama 240-8501
Phone: +81-45-339-4259 Fax: +81-45-338-1157 E-mail: yoshi@yoshilab.dnj.ynu.ac.jp

1. Introduction

Single-Flux-Quantum (SFQ) integrated circuits have the potential to achieve logic operation with clock frequency beyond hundreds of gigahertz and extremely low power consumption smaller than $10^{-8}$ w/gate at 50 GHz [1]. The main building circuit elements in the SFQ digital circuits are generally synchronously clocked gates, in which logical ones and zeros are represented by the presence or absence of an SFQ pulse within timing windows determined by periodic SFQ pulses. Precise timing design is, however, challenging because the delay in the clock distribution tree is comparable to the clock period in such high clock frequencies.

We have designed an eight-bit SFQ microprocessor to confirm feasibility of the large-scale SFQ digital system operating at high frequencies. Some new circuit architectures and circuit design methodologies are developed to overcome the difficulty in the timing design in the large-scale SFQ logic circuits. In this paper we will show the detail of our microprocessor design to show our new concept in the large-scale SFQ digital system design. Some key circuit components are implemented by using the Hypse 3.5 μm and NEC 2.0 μm Nb superconducting IC processes and their correct operations are confirmed.

2. Microprocessor Architecture

The designed processor consists of a one-bit ALU accompanied with two 8-bit registers (REG0 and REG1), an 8-bit instruction register (IR), a five-bit program counter (PC), a packet switch (PSW), a state controller (Controller) and a 32-byte register file (RAM) as shown in Fig. 1. The number of the instruction set is seven and address space is 32-Byte.

A bit-serial architecture, where data are processed as a serial data packet, is used to hide latency of logic blocks compared with the system cycle time at high local clock frequency. Though the system cycle time is slowed down in the bit-serial architecture, hardware complexity and size are reduced extremely. Therefore we can say that high local clock speed of SFQ circuits is utilized to reduce a hardware complexity in our design concept [2].

A distributed local clock architecture, where each register unit has its own local clock generator, and data-driven self-timing [3], where data themselves have their timing information, are also employed in the circuit blocks design to decrease the difficulty in globally synchronous timing design.

In the logic gate level, we used the asynchronous SFQ logic circuit based on the binary decision diagram (BDD) [4]. In this design approach, BDD graphs representing some logical functions are directly implemented by the simple SFQ gate, which is called Bina in our standard cell library. The important features of the BDD SFQ logic circuits are a small primitive number, non-clocked or asynchronous logic style, and a small gate count.

Fig. 1 A block diagram of the 8-bit BDD SFQ microprocessor based on a bit-serial architecture.

3. Circuit Design Methodology

We have developed a cell-based design methodology [5, 6] and prepared a top-down CAD environment to design large-scale SFQ integrated circuits [5]. In our design approach, logic circuits can be constructed by simply placing the tile-shaped basic cells. The design flow consists of five steps: logic synthesis by the BDD, schematic view entry, logic level simulation by Verilog-XL, circuit simulation by using Josephson circuit simulator, JSIM, and layout extraction from the schematic view by using the layout view library. CAD
tools for the top-down design flow and the BDD SFQ standard cell library have been integrated on the Cadence CAD environment.

4. Circuit Implementation and Test Results

The microprocessor is implemented by using the Hypres and NEC Nb superconducting IC processes. The target clock frequencies are 10 GHz and 16 GHz, for Hypres and NEC processes, respectively. Figure 2 shows a chip layout of the 8-bit BDD SFQ microprocessor using the Hypres process. The total Josephson junction number is about 5000. We confirmed complete operation of the system with sufficient timing margin by the logic simulation.

Some important circuit blocks, including the one-bit ALU, the eight-bit register and the packet switch have been tested and their correct operations have been confirmed. Figure 3 shows an example of the test results of the one-to-two packet switch. It switches the serial data packet from the input node (IN) into one of two output nodes (OUT1 and OUT2) depending on the selection input (S0 and S1).

On-chip high-speed test [7] of the 8-bit shift registers shows that the registers operate correctly at 10 GHz.

Fig. 2 A chip layout of the 8-bit BDD SFQ microprocessor using the Hypres Nb superconducting IC process. A Chip size is 10 mm x 10 mm.

5. Conclusions

We have designed an 8-bit SFQ microprocessor and confirmed correct operation of some circuit blocks. It is verified from the logic simulation that the system can operate at 10 GHz local clock frequency with sufficient bias current margin assuming the Hypres 3.5 μm superconducting IC process. It should be noted here that because the speed of the superconducting circuit proportionally increases with decrease of Josephson junction size, a local clock frequency beyond a hundred gigahertz is possible using a future superconducting IC technology with submicron Josephson junction size.

References