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High-speed Operation of a Single-Flux-Quantum (SFQ) Cross/bar Switch up to 35 GHz

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1. Introduction

The spread of broadband communication all over the world has increased the amount of data traffic on the Internet. A high-throughput packet switch is inevitable to avoid the bottlenecks in broadband networks of the future. To enhance packet-switch throughput, conventional semiconductor devices have been improved. However, they are facing power and speed problems. Namely, as the device size has been decreasing to achieve much higher speed, more power is consumed in a smaller area, leading to higher heat density on a chip. In return, higher heat density demands more space and longer wires between logic gates. Consequently, larger wiring delay limits circuit speed.

In these circumstances, single-flux quantum (SFQ) technology [1] is a novel technology that solves both problems. SFQ digital circuits can operate at high speed (up to several hundred gigahertz) with low power consumption. Typical power consumption per bit is below 10 nW at 1 GHz. This is a major advantage of SFQ technology over conventional semiconductor or other logic circuit technologies. Therefore, we believe that SFQ technology is a key to meet the demands of the rapid increase in data traffic. We have already developed an SFQ packet-switch architecture [2]. That realizes higher throughput by means of SFQ switch components that operate faster than the peripheral ones. The current paper presents the design and high-speed on-chip test results on a cross/bar switch, which is the core data path component in the SFQ packet-switch architecture.

2. Circuit design

2.1 Cell-based design method

A full-custom design method is commonly used for SFQ circuits. This is mainly because the target circuits are small or simple. On the other hand, to design general and large-scale SFQ circuits of the future, we use the cell-based design method. We have developed a CONNECT (cooperation of Nagoya University–NEC–CRL teams) cell library that comprises more than 100 standard cells

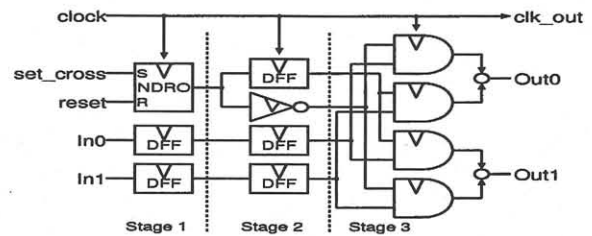


Fig. 1: Schematic of the cross/bar switch. DFF: D flip-flop, NDRO: Non-Destructive Read-Out.

[4]. Each CONNECT cell consists of a symbol, a digital behavior model, an SFQ circuit schematic, and a physical layout. The digital behavior model enables us to simulate a large-scale circuit at the digital level. Therefore, it is easy to expand the circuit size. Using the CONNECT cell library, we designed and demonstrated a large-scale SFQ logic circuit with about 730 cells and 2400 Josephson junctions [3].

2.2 Cross/bar switch circuit

To demonstrate high-speed operation of an SFQ logic circuit and its application to our switch architecture, we designed a cross/bar switch (Fig. 1). This switch is the main data-path component in the switch architecture. Input signals at *set_cross* and *reset* changes its state to “cross” and “bar,” respectively. In “bar” state, *In0*–*Out0* and *In1*–*Out1* are connected respectively, while in “cross” state, the connection is vice versa.

The switch consists of 13 logic gates (or cells) and three pipeline stages as shown in Fig. 1. In general, each SFQ logic gate, such as an AND gate, or an OR gate, has an internal memory that can be used as a pipeline register. Therefore, a gate-level deep pipeline is a natural result that can increase the throughput of the whole circuit to that of a single logic gate.

SFQ logic cells are connected by wiring cells whose propagation delay is comparable to the logic-gate delay. Therefore, a synchronous clocking scheme is impractical. A concurrent flow-clocking scheme is an asynchronous clocking scheme, where clock and data signals are distributed in the same direction as shown in Fig. 1. To

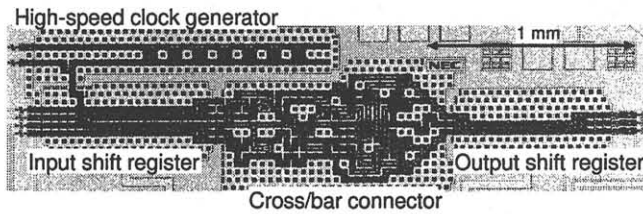


Fig. 2: Microphotograph of the cross/bar switch in the on-chip test system.

achieve high-speed operation, it is necessary to adjust data and clock propagation delays between logic gates. We placed wiring cells between logic gates, calculated propagation delays, and adjusted them by means of replacing wiring cells. In the cell-based design method, delay calculation is just the sum of cell delays on a signal propagation path; no dynamic simulation is required.

After timing adjustment, 194 cells and 581 Josephson junctions were used in the layout. We confirmed its correct switching operations up to 33 GHz in simulation.

3. Testing

3.1 On-chip test system

An on-chip test is inevitable to demonstrate high-speed operation over 10 GHz. An on-chip test system typically consists of a high-speed clock generator and input/output shift registers. We used our already developed standard cells for building these on-chip test components [5].

Figure 2 shows a microphotograph of the cross/bar switch in the on-chip test system. The length of the input and output shift registers is four bits each: the maximum test pattern length. The components used for the on-chip test consist of 598 Josephson junctions and 111 cells. Including I/O circuits, the whole system consists of 1236 Josephson junctions and 314 cells. The test chip was fabricated by using an NEC standard Nb process. The minimum junction size is $2\ \mu\text{m} \times 2\ \mu\text{m}$.

The system operates as follows. *Load*: An input test pattern is loaded into the input shift register from the off-chip pattern generator at low speed (several kilohertz). *Execution*: Triggered by an external signal, the high-speed clock generator produces a train of clock signals, which pushes data in the input shift register. After the circuit under test executes a logic operation on the data at high speed (over 10 gigahertz), the test results are stored in the output shift register. *Acquisition*: The results in the output shift register are sent to an off-chip measurement device at low speed.

3.2 High-speed on-chip test results

Figure 3 shows the observed waveforms. The top six waveforms are input signals. A rising edge corresponds to application of an SFQ signal. The bottom three waveforms are output signals. Either a rising edge

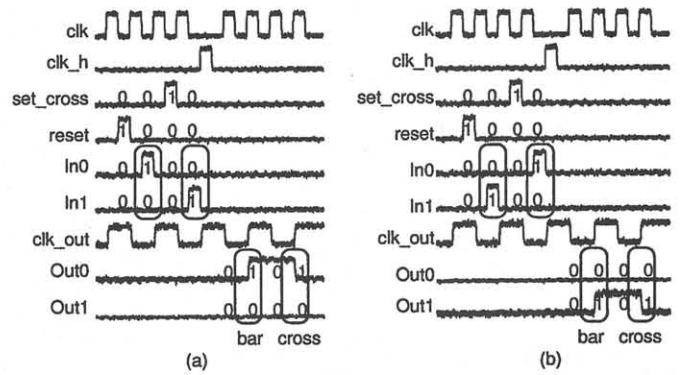


Fig. 3 High-speed on-chip test results.

corresponds to the observation of an SFQ signal.

First, we loaded a test pattern into the shift register: $\text{set_cross}=0010$, $\text{reset}=1000$, $\text{In0}=0100$, and $\text{In1}=0001$ with four clock signals. This means that the circuit receives data $(\text{In0}\ \text{In1})=(1\ 0)$ in "bar" state and $(\text{In0}\ \text{In1})=(0\ 1)$ in "cross" state. Then the test system was triggered by clk_h . After the cross/bar switch operated at high speed, the stored data was sent to the off-chip device with four clock signals. The results were $\text{Out0}=0101$ and $\text{Out1}=0000$ as shown in Fig. 3(a). Figure 3(b) is another high-speed test result, showing that Out1 also operates correctly.

The clock frequency of the high-speed clock generator depends on the bias current supplied to it. By changing the current, we confirmed correct operation of the switch up to 35 GHz, close to the maximum frequency in simulation.

4. Conclusions

We designed a cross/bar switch by using a cell-based design method. It was experimentally showed that the cross/bar switch in the on-chip test system can operate up to 35 GHz. This result demonstrates high-speed operation of SFQ logic circuits and the efficiency of the cell-based design method.

Acknowledgments

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