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A Fine-Grained Programmable Logic Module with Small Amount of Configuration Data for Dynamically Reconfigurable Field Programmable Gate Array (FPGA)

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1. Introduction

Dynamically customizable and reconfigurable hardware architecture for a specific task on demand is one of the most important issues to bring out a novel-computing paradigm in the era of system LSI [1]. Multi-context field programmable gate array (FPGA) is a leading candidate of the dynamically reconfigurable processor [2]. However, similar to the conventional FPGA, if the size of target application exceeds the usable gate capacity of FPGA, it cannot operate at all. The adaptive field of the reconfigurable computing is limited. It is therefore necessary to read configuration data (CD) from off-chip memory in order to remove this constraint. Since the amount of CD is enormous in the conventional FPGA consisted of Look Up Table (LUT), data transfer time is too long to do reconfiguration in real time. Therefore, not only raising data transfer rate but also reducing CD amount is necessary for speeding up the dynamic function switching.

In this paper, we proposed a new programmable logic module for dynamically reconfigurable FPGA which makes it possible to significantly reduce CD amount required for logic generation in various applications to about 1/7 as compared to the conventional LUT-based logic module. Unlike LUT-based conventional module, programmable functions of the proposed module are carefully selected with preserving essential functions for logic synthesis, while redundant functionality is eliminated.

2. Newly Developed Programmable Logic Module

The schematic diagram of newly developed fine-grained programmable logic module is shown in Fig. 1. This module is composed of 3 parts. The first part is the advanced Full-adder/D-flip-flop Merged Module (FDMM) (Fig. 2). The original FDMM is a kind of programmable logic module for only datapath applications [3]. In order to adapt to general-purpose applications using electrical design automation, advanced FDMM can act as either Full-adder or D-flip-flop with asynchronous initialization. Full-adder in the FDMM realizes some useful functions, but it is not sufficient. Therefore, the second part consisted of 3 logical functions such as 4-input NAND, NOR and OR-AND-INVERTER is added as an additional logical part. These functions are carefully selected from thousands of possible logical functions in order to minimize the amount of CD most efficiently, especially for random logic applications. The last part is a selector, which decides the output of this module from functions of the first and the second parts by controlling "sel 0" and "sel 1".

3. Logic Synthesis Experiment

To confirm the efficiency of the newly developed programmable logic module, we made experiments on logic synthesis. It is necessary to assume the programmable routing architecture and benchmark circuits for the experiment. As routing architecture, we assumed the sea-of-gate model with 32:1 multiplexer per single input and 3-state buffer per single output. This has enough ability to place and route each netlist completely. And we picked up applications categorized to datapath, microprocessor and random logic as benchmark circuits in order to ensure the generality of the newly developed module (Table I).

4. Results and Discussion

Fig. 3 and 4 shows the cell counts, which is the number of the module used, and the amount of CD respectively that are necessary to generate the logic of each benchmark circuit using proposed programmable logic module and conventional 4-input LUT-based module. From the result, proposed module significantly lowered the amount of CD to about 1/7 as compared to LUT-based module without severe increase in cell counts. This indicates that the new module does actually reduce the amount of CD in spite of eliminating a lot of functions that LUT can realize.

Fig. 5 shows the total amount of CD required for realizing each benchmark circuit on the FPGA based on the proposed module and 4-input LUT-based FPGA. This is the sum of CD required for programmable logic module and programmable routing. Though the amount of CD for routing is much larger than that for logic module, total reduction rate of the whole FPGA improved over 30% by using the proposed module.

5. Conclusions

In this paper, we proposed the new programmable logic module. This module can significantly reduce the amount of CD necessary for logic synthesis, about 85% less than conventional LUT-based logic module.

Using this module, we have designed a dynamically reconfigurable FPGA. Layout of the chip is shown in fig. 6. With this chip, we make advance in the novel-computing, reconfigurable computing for large-scale applications.

Acknowledgments

The VLSI chip in this study was designed and is being fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Avant!, Synopsys and Cadence CAD tools and by Rohm Corporation and Toppan Printing Corporation.

References

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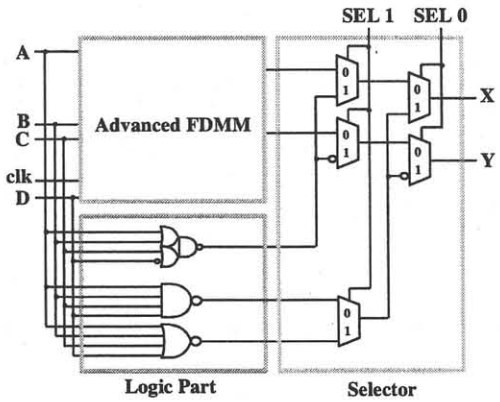


Fig. 1 The schematic diagram of newly developed programmable logic element for the dynamically reconfigurable FPGA

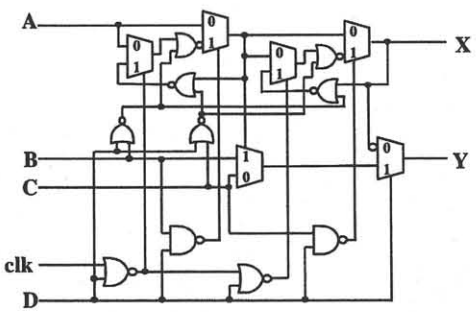


Fig. 2 The schematic diagram of advanced Full-adder/D-flip-flop Merged Module (FDMM)

Table I Experimental circuit characteristics

#	Circuit	Type
1	laplacian filter	datapath
2	gaussian filter	datapath
3	median filter	datapath
4	zoom block	datapath
5	stop watch	random logic
6	zoom controller	random logic
7	thermometer	random logic
8	viterbi decoder	random logic
9	popcorn	microprocessor
10	kue-chip2	microprocessor

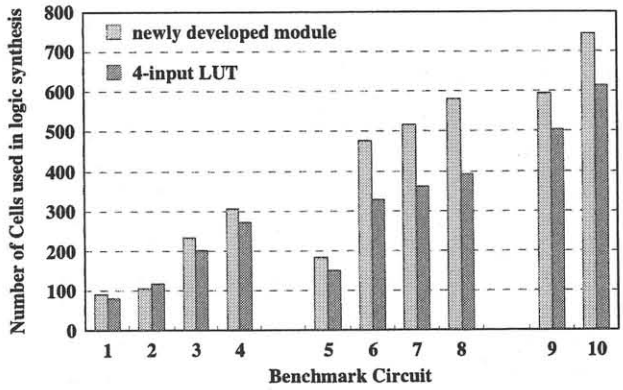


Fig. 3 Logic Synthesis result: Cell counts which is required in logic synthesis

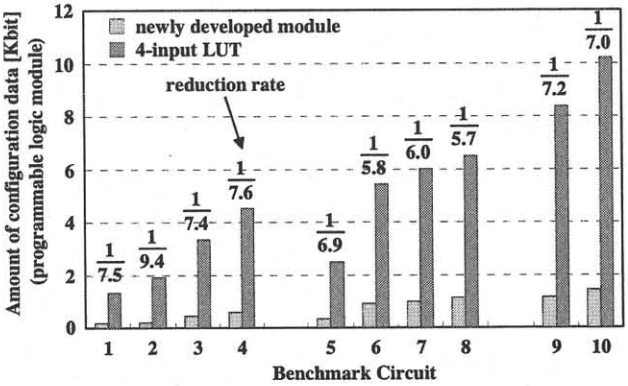


Fig. 4 Logic Synthesis result: configuration data of programmable logic module for logic generation

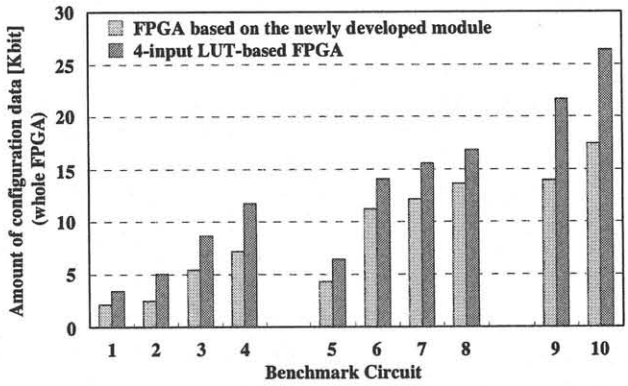
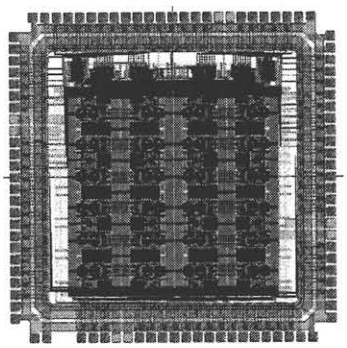


Fig. 5 Logic Synthesis result: total configuration data necessary for whole FPGA including routing information



Technology
CMOS 0.6um, 3-layer-metal

Chip Size
3.9mm×3.9mm
(about 0.2K usable gates,
4 context memory planes)

Fig. 6 The chip layout of the dynamically reconfigurable FPGA using newly developed programmable logic module