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Design and Implementation of Read-Compare-Write circuits for low power Multi-Gigabit DRAM

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ABSTRACT

This paper presents new data write circuits for low power DRAM and implements a 6Mb test DRAM with 0.16um CMOS process. The read-compare-write (RCW) circuits eliminate the redundant write operation that overwrites the same value to the cell. The adaptive column control (ACC) block assists the RCW operation and minimizes the column path activation. The RCW reduces the power consumption by maximum 24%.

1. INTRODUCTION

As the integration capacity of DRAM exceeds Gigabit and its operating speed reaches 1Gbps, its power consumption should be carefully examined. In addition, low power DRAM is essential requirement in recent mobile applications to extend their battery lifetime. In order to reduce power consumption, many techniques have been proposed such as single bit line writing [1], partial segment activation [2], sequential block activation [3], small voltage swing [4] and so on. These techniques have been focused only on the cell array or bit line operations.

In this paper, new writing circuits and scheme called RCW are proposed and a test chip is implemented for low power multi-gigabit DRAM. The proposed RCW circuit reduces overall DRAM power consumption up to 24% of conventional works according to data update ratio. The ACC circuit assists the proposed RCW circuit providing bitwise column activation. For the verification of the RCW circuit, a 6Mb DRAM is designed using 0.16μm CMOS technology. And its power consumption is analyzed for the various data update ratio.

2. READ-COMPARE-WRITE (RCW)

In conventional DRAM write operation, the write driver is always enabled whether the previous data is the same as the new data or not. The RCW operation, however, depends on the comparison result between the stored value and the newly write value. If two values are equal, the operation ends without overwriting the cell (non-update-write). Otherwise, the cell is updated in the similar way as the conventional write (update-write) operation. The DB driver for RCW is shown in Fig. 1 and the WEN generator circuit is shown in Fig. 2. WEN signal enables the write driver if the values of the read latch and the write latch are different from each other.

The column gate signal (cdi) is controlled by the ACC block as shown in Fig. 3. The proposed ACC block disconnects the BL from the DB when the update of BL is exempted by the RCW operation.

- NON-UPDATE WRITE – In read operation, the read data value is stored at the read latch with small voltage difference between DB and DB#. In write operation, the newly written value is stored at the write latch. At the same time, the WEN generator outputs the comparison result. When it is equal, the write driver is not activated, and the cdi signal is disabled by ACC block. During this operation, the bit line sense amp (BLSA) has the previous cell value and cdi is disabled after read operation. The cell still maintains the right value without incurring the large voltage swing on the DB line pair.
- UPDATE WRITE – The operations of read and write latch are the same as those of NON-UPDATE WRITE. However, since the comparison result is different, the write driver and the cdi are activated. The operations after comparison are the same as those of the conventional write scheme.

3. TEST DRAM AND POWER ESTIMATION

A 6Mb test DRAM with the proposed RCW circuits is designed using 0.16um DRAM process and its features are summarized in Table. I. Overall power consumption of the write operation is ranged from 47mW to 70mW according to data update ratio as shown in Fig. 6. Power consumption of the RCW scheme is proportional to the number of data bits that have to be overwritten, not the number of data bits. The power saving factor by the RCW scheme is further enhanced as the memory density and bandwidth are increased. This is because the increase in both DB load capacitance and the number of DB line enlarges the portion of DB power consumption out of the entire DRAM power dissipation, and it can be reduced by the proposed RCW scheme. This becomes true in recent multi-gigabit DRAM. Additional power consumption due to the RCW scheme, such as the ACC circuit and the comparison circuits, is 5.6%~15.7% of total power consumption.

4. CONCLUSION

The read-compare-write scheme is presented for multi-gigabit low power DRAM and a test DRAM is designed and implemented with 0.16um CMOS technology. Power consumption of the DRAM with RCW scheme, ranging from

76% to 113% of the conventional scheme, is proportional to the number of data bits to be overwritten, not the number of all data bits. The area increase for RCW is less than 5%. The power saving factor by the RCW scheme is further enhanced as memory density and bandwidth are increased, such as multi-gigabit DRAM.

REFERENCES

[1] Jeonghoon Kook and Hoi-Jun Yoo, "A Single Bit line Writing Scheme for Low Power Reconfigurable I/O DRAM Macro", IEEE European Solid-State Circuit Conference, pp.420-423, Sept. 2000.

[2] Sugibayashi, T. et al., "A 30ns 256Mb DRAM with Multi-Divided Array Structure", Dig. Of Technical Paper, International Solid-State Circuits Conference, pp.50-51, 1993.

[3] Y. H. Park, et al., "A 7.1GB/s Low-Power 3D Rendering Engine in 2D Array-Embedded Memory Logic CMOS," IEEE J. Solid-State Circuits, vol. 36, pp.944-955, June 2001.

[4] Aimoto, Y. et al., "Design of 1024-I/Os 3.84GB/s High Bandwidth 600mW Low Power 16Mb DRAM Macros for Parallel Image Processing RAM", IEICE Trans. Electron., pp. 759-767, May 1998

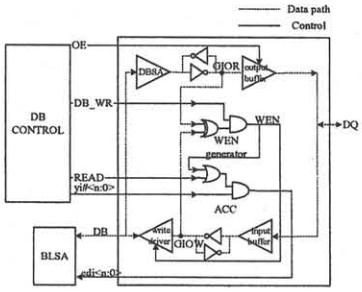

Fig. 1 DB driver

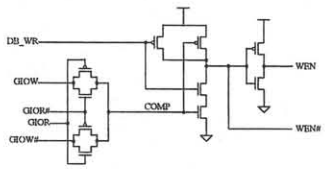

Fig. 2 WEN generator

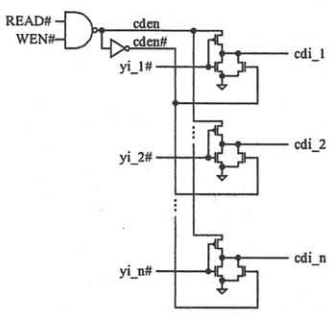

Fig. 3 ACC schematic

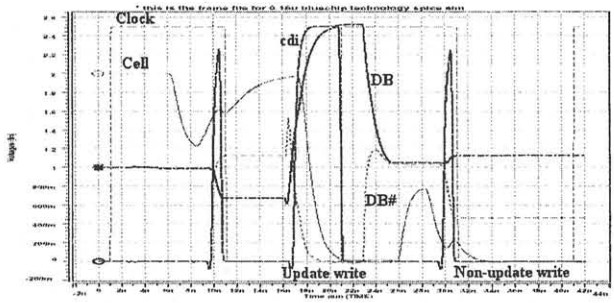

Fig. 5 Waveform of RCW operation

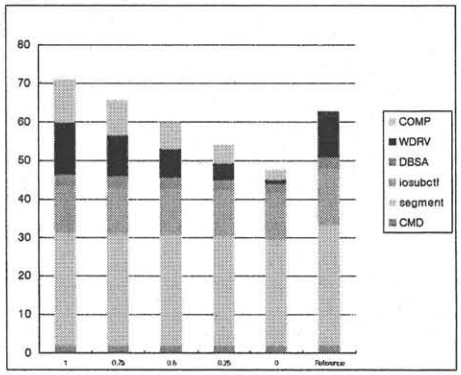

Fig. 6 Power consumption of the proposed RCW scheme and the conventional scheme

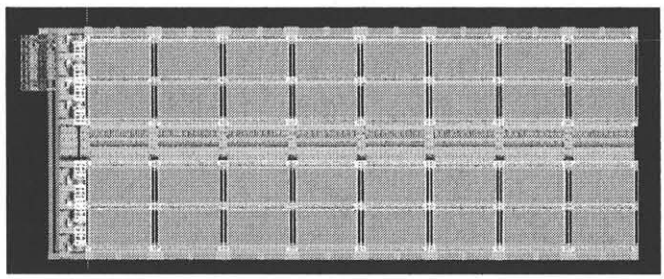

Fig. 7 Die micrograph of 6M eDRAM

Table. I eDRAM features

Technology	0.16um DRAM
Supply Voltage	2.0/2.5/3.5V(core/peri/Vpp)
I/O	192
Clock Frequency	50MHz
tRC	20ns
Peak Bandwidth	9.6GB/s
Power	47mW(data update ratio = 0.0) 70mW(data update ratio = 1.0)