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Optimum Device Consideration for Standby Power Reduction Scheme Using Drain Induced Barrier Lowering (DIBL)

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1. Introduction

The rapid increase in standby leakage power is one of the most critical problems in advanced LSIs using scaled MOSFETs. It is well known that, when the drain voltage is applied in short channel MOSFETs, threshold voltage (V_{th}) decreases due to drain induced barrier lowering (DIBL) effect [1], resulting in further increase in subthreshold leakage power. In order to suppress the standby power, several circuit schemes have been proposed including variable threshold voltage CMOS (VTCMOS) [2] and multiple threshold voltage CMOS (MTCMOS) [3]. However, it has been found that the standby power reduction scheme using VTCMOS is not scalable and an additional leakage is induced by substrate back-bias [4]. In the MTCMOS scheme, there is an area penalty, and memory data in SRAM and F/F are lost because the leakage current is completely shut off [5].

Recently, a new scheme for subthreshold leakage power reduction using DIBL has been proposed [6,7]. When the drain voltage, i.e. the supply voltage, is lowered in the standby mode, the DIBL effect is relaxed and V_{th} increases, thus reducing the standby leakage current. Although the standby power is not completely suppressed, this scheme is one of the simplest power reduction methods. Moreover, memory data are not lost. In this study, we investigate the optimum device for the standby power reduction scheme using DIBL by means of device simulation [8]. In particular, it is clarified whether the DIBL effect should be strong or not in the present scheme.

2. Standby Power Reduction Scheme Using DIBL

Fig. 1 shows a schematic of the DIBL effect. When the short channel effect is worse, V_{th} decreases more due to larger DIBL when large V_{ds} is applied, and off-current (I_{off}) increases. The scheme presented in this study utilizes this effect conversely. When the supply voltage (V_{dd}) is reduced in the standby mode, I_{off} is largely suppressed as shown in Fig. 1. Fig. 2 shows a typical V_{ds} dependence on V_{th}. V_{th} decreases almost linearly with increasing V_{ds}. The value of DIBL is usually defined as

$$DIBL = |\Delta V_{th}| / |\Delta V_{ds}|. \quad (1)$$

The typical value of DIBL in advanced MOSFETs is about 100 mV/V [9]. The values of V_{th} at V_{ds} = 0.1V and 1.2V are taken to derive ΔV_{th} in this study.

To examine the optimum device for this DIBL scheme, on-current (Ion) is set constant and I_{off} is compared at different V_{ds} in this study. A single nMOS device, instead of stacked devices [7], is investigated. In order to change the DIBL value in a wide range, a device with an ideal step-shape profile is assumed, as shown in Fig. 3. Changing depth and concentration of the upper layer (t_d), the depletion layer width (hence DIBL) and V_{th} can be independently changed [10]. Device parameters assumed are summarized in Table 1, which is based on the 130 nm technology node in ITRS [11]. Fig. 4 shows the t_d dependence of DIBL. When t_d (i.e. depletion width) is larger, the short channel effect is worsened resulting in larger DIBL.

3. Simulation Results

Fig. 5 shows the dependence of I_{off} on DIBL and V_{ds} in high performance (HP) devices at fixed Ion of 900 μA/μm. When V_{ds} equals to V_{dd} (1.2V), i.e. the DIBL scheme is not utilized, I_{off} first decreases and then increases with increasing DIBL, and I_{off} has the minimum value at a certain DIBL (at 80 mV/V). This result indicates that there are two competing factors that decrease and increase I_{off}. The former would be the DIBL dependence of current drive. It is reported [1] that current drive increases with increasing DIBL due to relaxed vertical field. In the present simulation, I_{on} is fixed, and therefore, I_{off} decreases with increasing DIBL. The latter is caused by the S factor degradation. Fig. 6 shows the DIBL dependence of S factor. As DIBL increases, S factor severely increases and I_{off} increases.

When V_{ds} is reduced, i.e. the DIBL scheme is utilized, I_{off} significantly decreases as shown in Fig. 5. As expected, the current reduction ratio increases with increasing DIBL, and the ratio reaches almost 100 when DIBL = 126 mV/V and V_{ds} = 0.1V. The S factor is also recovered at small V_{ds} (Fig. 6), and therefore I_{off} decreases monotonously with increasing DIBL, indicating that the effect of DIBL dependence of current drive [1] is dominant. It is interesting to note that, similar to VTCMOS [10], the critical drain voltage, V_o, can be defined when the two factors are competing: when $V_{ds} > V_o$, DIBL should be small to suppress I_{off}, while when $V_{ds} < V_o$, DIBL should be larger. This result indicates that the optimum device depends on how V_{ds} in the standby mode can be reduced.

Figs. 7 and 8 show the DIBL dependence of I_{off} and S factor in low power devices (LOP and LSTP), respectively. Since V_{th} is higher than HP devices, the depletion layer is thin and the short channel effect is better. Therefore, I_{off} decreases with increasing DIBL.

Finally, the effect of device fluctuations on power reduction is discussed. It is reported that VTCMOS with negative bias enhances the fluctuations of device characteristics [12]. Fig. 9 shows a typical L_g dependence of V_{th}. In the present DIBL scheme, the device with short L_g (hence higher I_{off}) can be more recovered by larger DIBL. Therefore, the fluctuations of I_{off} are suppressed using the DIBL scheme.

4. Conclusions

The optimum device for power reduction scheme using DIBL is discussed. By lowering the supply voltage in the standby mode, the standby power is reduced due to relaxed DIBL. It is found that there exists the critical drain voltage, V_o. When $V_{ds} < V_o$, larger DIBL is preferable to suppress I_{off}. It is also found that the fluctuations of off-current are suppressed using the DIBL scheme.

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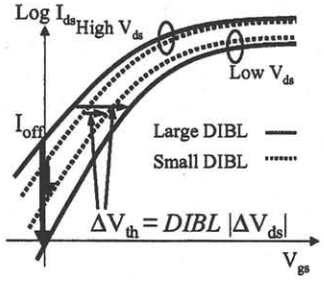

Fig.1. A Schematic of the DIBL effect. In a device with larger DIBL, off-current is more reduced when V_{ds} is low.

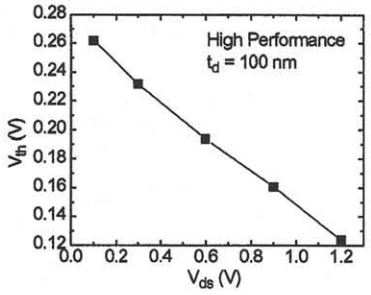

Fig.2. The typical V_{ds} dependence of V_{th}.

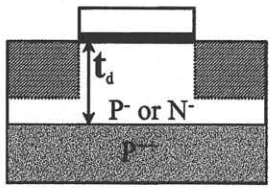

Fig.3. The device structure used in the simulation. An ideal step impurity profile is assumed.

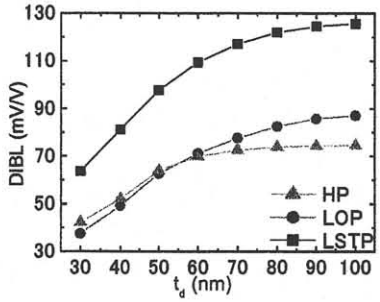

Fig.4. The dependence of DIBL on t_d.

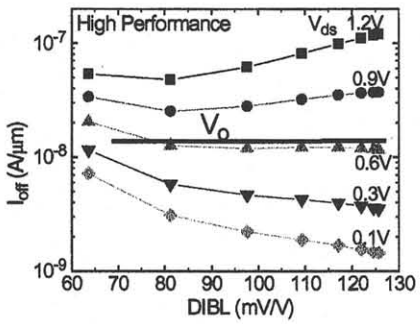

Fig.5. DIBL dependence of I_{off} in high performance devices. The critical drain voltage, V_o, can be defined. When $V_{ds} < V_o$, DIBL should be larger to suppress I_{off}. On the other hand, DIBL should be small when $V_{ds} > V_o$.

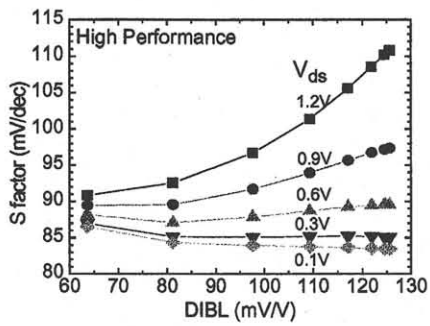

Fig.6. DIBL dependence of S factor in high performance devices. The S factor is improved when V_{ds} is reduced.

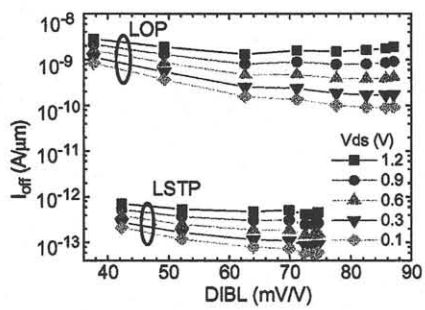

Fig.7. DIBL dependence of I_{off} in low power devices (LOP and LSTP). I_{off} decreases with increasing DIBL, because S factor degradation is not significant in low power devices (see Fig. 8).

Table 1. Parameters assumed in the device simulation. The parameters are based on the 130 nm node in ITRS [11].

Technology requirements	HP	LOP	LSTP
	High Perform-ance	Low Operating Power	Low Standby Power
I_{on} (μA/μm)	900	600	300
Physical gate length (nm)	65	90	90
T_{ox} electrical equivelent (nm)	2.3	3.0	3.4
V_{dd} (V)	1.2	1.2	1.2

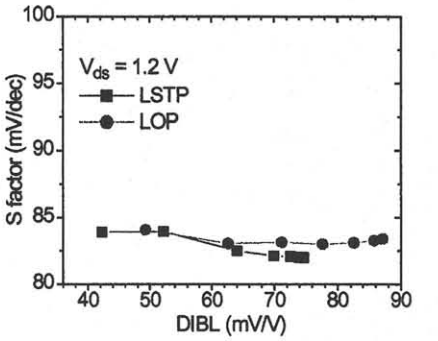

Fig.8. DIBL dependence of S factor in low power devices.

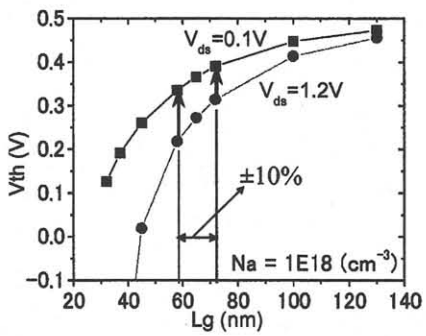

Fig.9. L_g dependence of V_{th} at V_{ds} = 1.2 V and 0.1 V. The typical L_g is 65 nm and it is assumed that it varies in the range of ± 10%. The fluctuations of I_{off} can be suppressed in the present DIBL scheme because a device with worse short channel effect is more recovered