Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 782-783

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Ultra Thin Body Silicon-On-Insulator (UTB SOI) MOSFET with Metal Gate Work-function Engineering for sub-70 nm Technology Node

Daewon Ha, Pushkar Ranade, Yang-Kyu Choi, Jeong-Soo Lee, Tsu-Jae King, and Chenming Hu

University of California at Berkeley, Department of Electrical Engineering and Computer Science
373 Cory Hall, University of California, Berkeley, CA 94720, USA
Phone: +1-510-643-2558 Fax: +1-510-643-2636 E-mail: daewon@eecs.berkeley.edu

1. Introduction

Fully depleted ultra-thin-body (UTB) SOI MOSFET structures provide excellent suppression of short channel effects and hence are promising for sub-70nm technology [1],[2]. However, it is very difficult to adjust the threshold voltage (V_T) of a UTB MOSFET by conventional channel implantation [3]. To avoid dopant fluctuation effects, a lightly doped Si body should be used, with threshold voltage adjustment achieved via gate work-function engineering. Metallic gate materials are desirable for reducing resistance, and for eliminating the gate depletion effect as well as dopant penetration through ultra-thin gate dielectrics. In this paper, threshold voltage adjustment for Mo-gated UTB MOSFETs by nitrogen implantation is demonstrated for the first time.

2. Device Fabrication

Fig.1 summarizes the sequence of process steps used to fabricate UTB MOSFETS in this work, and Fig.2 provides a cross-sectional schematic of the final structure. The initial SOI film (p-type, 15Ω-cm, <100>, T_{Si}/T_{BOX}=100nm/400nm) was thinned down to ~10nm by thermal oxidation. The body thickness was chosen not to be too thin, to avoid V_T shifts due to quantum confinement [4]. After active-area patterning, the gate dielectric was formed by thermal oxidation (2.5nm) and the Mo gate film (40nm) was deposited in a DC magnetron sputtering system at 200°C (10^{-7} Torr base pressure). Then, nitrogen implantation was performed at various doses (see Table I for experimental split conditions). N+ poly-Si and a SiO_2 hard-mask layer were then deposited. The purpose of the hard mask was to prevent shorting of the source and drain (S/D) during the subsequent selective deposition of Ge to form raised S/D contact regions (Fig. 2). A highly selective dry etch process (selectivity > 70:1) was developed to etch the Mo gate on thin gate oxide. After gate-sidewall spacer formation, Ge was deposited selectively and S/D implants were performed. Device fabrication was completed with a 60s, 700°C RTA in N_2 ambient to activate the implanted S/D dopants. This conservative anneal was used because Ge and Si intermixing is known to be enhanced in the presence of dopants [6], for the formation of abrupt and shallow pn junctions with low thermal budget.

3. Results and Discussion

Fig.3 shows the measured high-frequency C-V curves for bulk-Si control devices implanted with various doses of $^{14}N^+$ (Table I). The shift in flat-band voltage V_{FB} is proportional to the implant dose (ΔV_{FB} = 65mV/1x10^{15} cm^{-2}). Since nitrogen diffuses rapidly in Mo and segregates to the Mo-SiO_2 interface [5], the concentration of nitrogen at the interface is dependent on the total nitrogen dose implanted inside the Mo film. Fig.4 shows XRD analysis results for two different samples. The sample implanted with nitrogen shows several diffraction peaks corresponding to Mo_2N. This is evidence that Mo is chemically modified to Mo_2N at the interface, to effect a reduction in gate work-function.

V_T was extracted for the UTB MOSFET using the $g_{m,max}$ method, as shown in Fig.6. The Mo-gated PMOS V_T is –0.2V, and shifts by approximately -65mV for every 1x$10^{15}$$cm^{-2}$ increment in $^{14}N^+$ implant dose (Fig.7). Thus, the threshold voltage of UTB MOSFETs can be effectively adjusted via gate work-function engineering. In order to achieve the desired V_T (0.2~0.3V) in n-channel UTB MOSFETs, and estimated dose of 6~8x10^{15} cm^{-2} is needed. Fig.8 shows measured DIBL for UTB PMOSFETs. Despite the lightly doped ($10^{15}$$cm^{-3}$) body, DIBL is greatly suppressed (< 40mV/V) because of the ultra-thin body.

4. Summary

Metal gate work-function engineering is demonstrated to be feasible for adjusting the V_T in UTB SOI MOSFETs, for the first time. Mo gate technology is an attractive candidate for future CMOS technologies employing UTB MOSFET structures, particularly for multiple-V_T applications.

Acknowledgement

This work is supported from the MARCO Focused Research Center on Materials, Structures, and Devices which is funded at the Massachusetts Institute of Technology, in part by MARCO under contract 2001-MT-887 and DARPA under grant MDA972-01-1-0035. The authors would like to thank the staff of the Microlab in University of California, Berkeley.

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Table I. Process split conditions

	Initial WF	$^{14}N^{+}$ Implant Condition
Ctrl 1	Bulk P-type $<10^{15}$ cm^{-3}	No Implant
Ctrl 2		20KeV, $2x10^{15}$cm^{-2}
Ctrl 3		20KeV, $4x10^{15}$cm^{-2}
Smpl 1	UTB SOI P-type (10^{15}cm^{-3})	No Implant
Smpl 2		20KeV, $2x10^{15}$cm^{-2}
Smpl 3		20KeV, $4x10^{15}$cm^{-2}

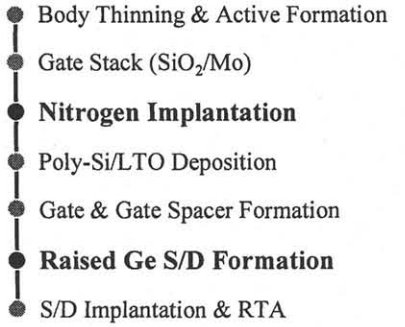


Fig. 1 Sequence of fabrication steps for UTB SOI MOSFET.

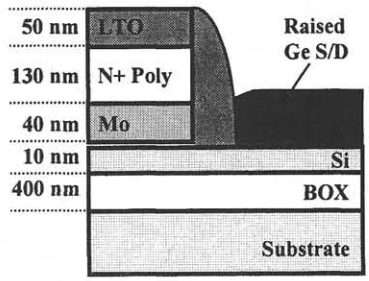


Fig. 2 Cross-sectional schematic of the final UTB SOI MOSFET.

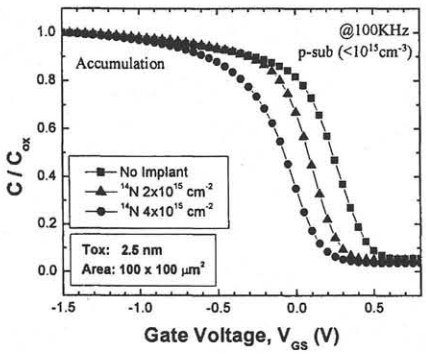


Fig. 3 Measured high-frequency CV curves of bulk-Si control devices after RTA.

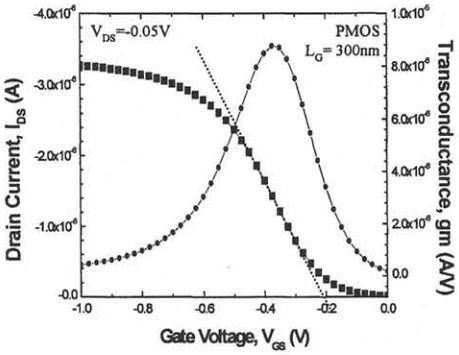


Fig. 5 The $g_{m,max}$ method was used to extract the V_T of UTB MOSFET.

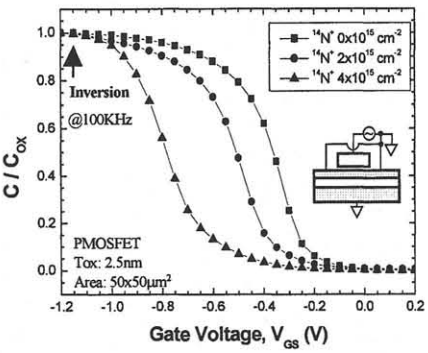
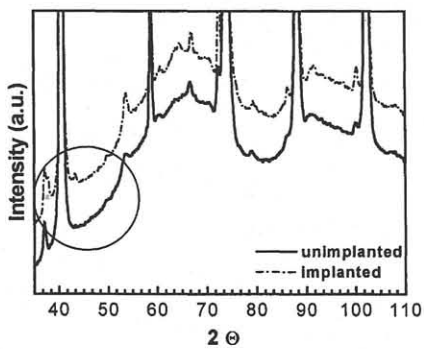
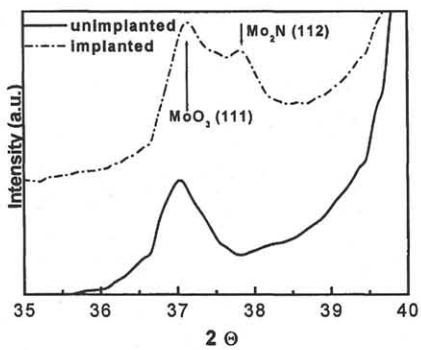


Fig. 6 Measured high frequency CV curves for UTB capacitors. (V_T=-0.2, -0.32, -0.6)





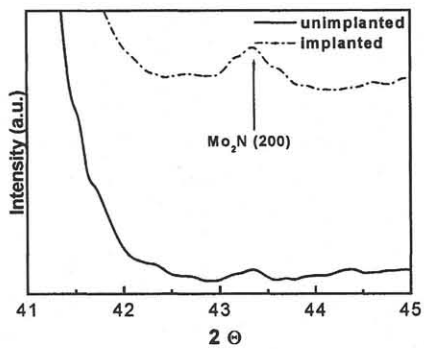


Fig. 4 XRD analysis of Mo gate films. (a) The entire range of peaks, (b),(c) details of XRD peaks. The peaks indicate that Mo_2N is formed in the nitrogen implanted sample.

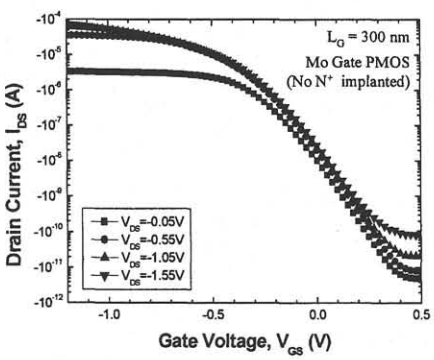


Fig. 7(a) I_{DS}-V_{GS} characteristic of UTB PMOSFET.

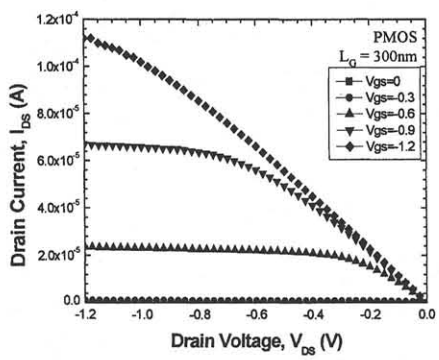


Fig. 7(b) I_{DS}-V_{DS} characteristic of UTB PMOSFET.

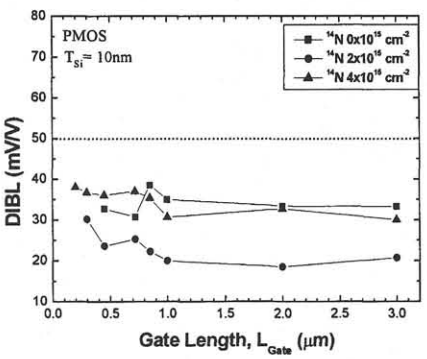


Fig. 8 DIBL is suppressed below 40mV/V due to the ultra thin body.