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Body Potential Design Using Narrow and Shallow Halo to Reduce the Floating Body Effect of SOI-MOSFET

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Abstract

A body potential design using narrow and shallow halo is proposed to reduce the floating body effect in the moderately thin SOI-MOSFETs. A 0.1 μm gate length and 50nm thick SOI-MOSFET was fabricated based on the method. A reduction in the floating body effect is demonstrated by the device.

1.Introduction

Small parasitic capacitance in the SOI-MOSFET is attractive for high speed and low power LSI's. However, the floating body effect, in which excess majority carriers induce the abnormal drain current, is a drawback of the device[1]-[4]. As the devices are miniaturized, increased channel doping leads to a larger barrier height (E_{barri}) for majority carrier diffusion, and it becomes difficult to fabricate a fully depleted (FD) SOI-MOSFET having an E_{barri} small enough to suppress the floating body effect. Although an ultra thin SOI structure is a possible solution for the problem, it requires complex fabrication process such as epitaxital growth for source/drain formation.

Therefore, we propose a body potential design method to reduce the floating body effect of moderately thin SOI-MOSFET (typically 30-50nm, bulk-compatible S/D formation is applicable). The impact of the halo width control and halo depth control on E_{barri} is investigated using device simulation. Based on the result, an SOI-MOSFET having a steep and shallow halo was fabricated by using low energy halo implantation and a spike (short time) anneal process. The device demonstrated the effectiveness of the method for reducing the floating body effect.

2. Simulation

The barrier height for the majority carrier diffusion (E_{barri}) is calculated over various halo width (d), for L=0.1 μm and T_{SOI}=50 nm SOI-MOSFETs (Fig. 1 (a)). It is found that E_{barri} decreases with d decreasing. Fig.2 shows the difference between surface potential (having an influence on V_{TH}) and back interface potential (having an influence on E_{barri}) of the SOI layer, for various halo width. Figure 2 clearly shows that the potential depth in the back interface, i.e., the barrier height for majority carrier diffusion, decreases in a narrow halo device.

Fig.1(b) shows the E_{barri} dependence on the halo depth. A shallow halo is effective to reduce E_{barri}, since the halo impurities, which lower the body potential, do not exist near the back interface. However, Fig.3(a) shows that a very low impurity concentration under halo makes the back interface potential higher than surface potential in the halo region. A moderate doping under halo is preferable (Fig.3 (b)) to avoid the punch through at the back interface.

Subthreshold characteristic for a device having a narrow and shallow halo and a moderate under-halo-doping (Fig.4(b)) are simulated. V_{TH} lowering due to the floating body effect is suppressed in the device, since a small E_{barri} prevents majority carriers (hole) from accumulating in the body.

3. Experiment

Based on the above investigation, a 50nm thick SOI-MOSFET with narrow and shallow halo are fabricated. A low energy and large tilt angle halo implantation and a spike (fast rump-up, zero-hold and fast rump down) annealing[5] were adopted. The channel implantation energy is also reduced to obtain steep impurity profile. Simulated impurity profile of the device (Fig.5) is clearly different from that of the control device using conventional rather broad halo implantation and conventional RTA process.

Figure 6 shows the V_{TH} dependence on the substrate (under buried oxide) voltage (V_{sub}) at V_D=0.05V. The conventional device show a flat behavior which is characteristic in partially depleted (PD) device. E_{barri} of the device is large enough to form a neutral region in the body. Therefore, the majority carriers (hole) accumulates in the neutral region and induce a large drain current kink, as shown in Fig.7 (a). However, the proposed device shows the fully depleted (FD) characteristic in which V_{th} depends on V_{sub} (solid circles in Fig.6). A small E_{barri} in FD device enhances the diffusion and recombination of hole, and consequently, the drain current kink is reduced, as shown in Fig.7 (b).

4. Conclusions

From a systematic simulation, it was found that a narrow and shallow halo is effective to reduce majority carrier accumulation. A 0.1 μm SOI-MOSFEFT demonstrated the impact of the method..

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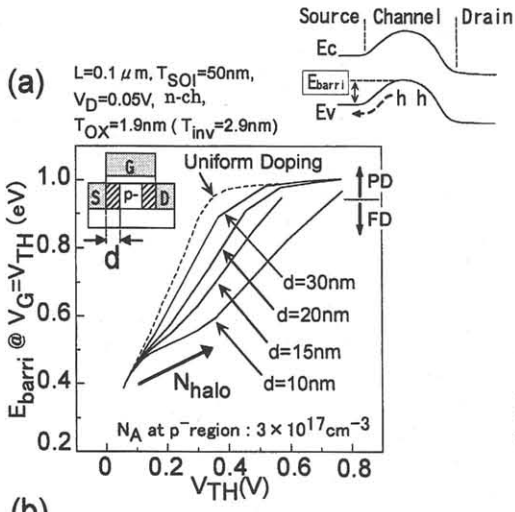

Fig.1 E_{barri} dependence on V_{TH}

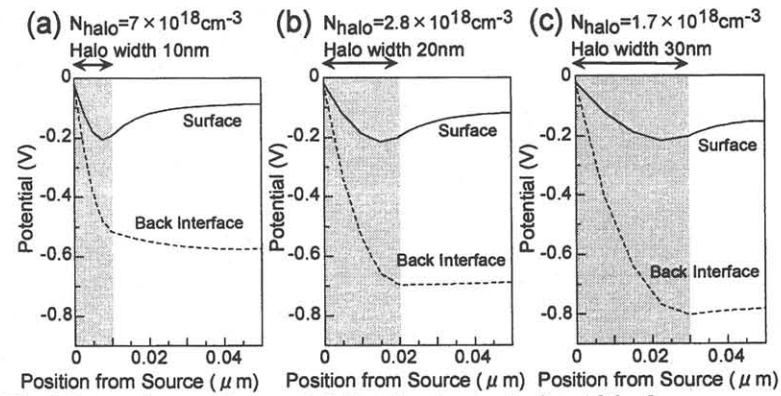

Fig.2 Dependence of potential distribution on halo width d, at V_G=-0.2V, V_D=0.05V. SOI Thickness is 50nm and L is 0.1 μm.

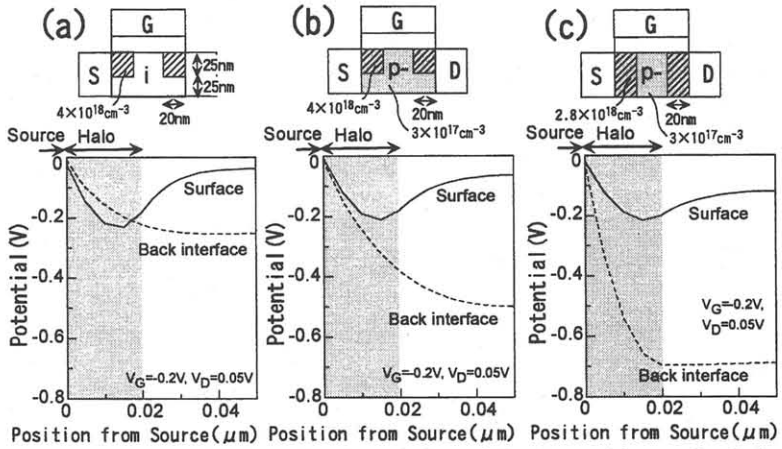

Fig.3 Influence of the halo depth and that of the impurities under halo.

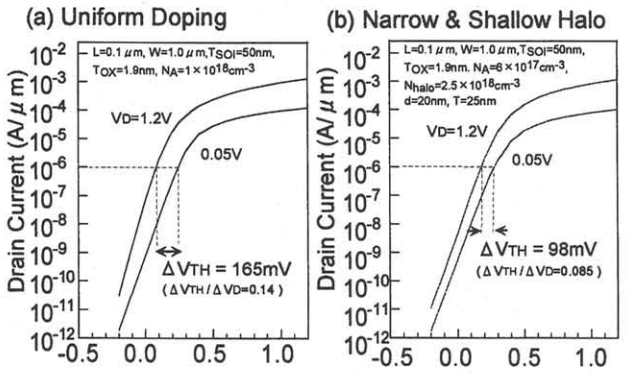

Fig.4 Suppression in the floating body induced V_{TH} variation.

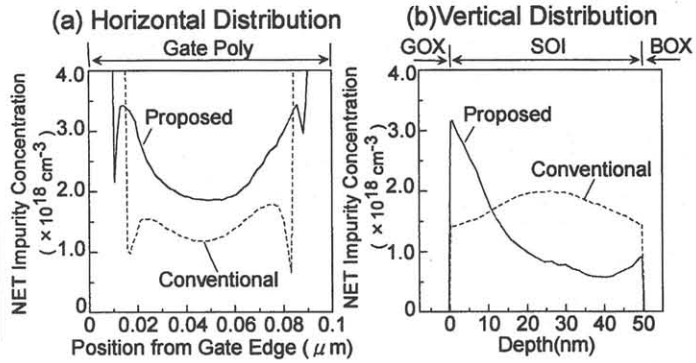

Fig.5 Simulated impurity distribution of fabricated device. SOI Thickness is 50nm and L is 0.1 μm.

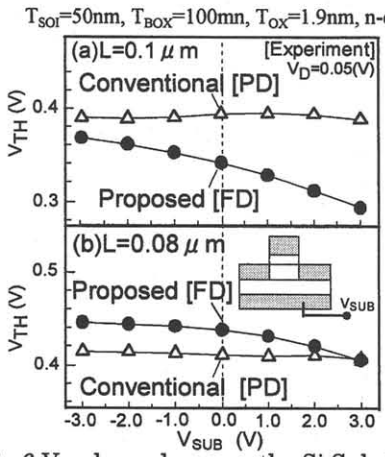

Fig.6 V_{TH} dependence on the Si Substrate.

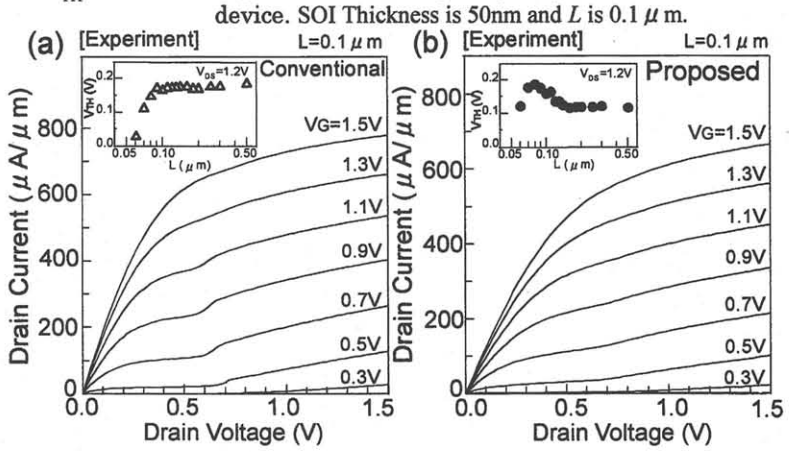

Fig.7 Reduction in the floating body induced kink.