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High Performance Poly-Si CMOS Circuits Fabricated Using Metal Imprint Technology

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1 Introduction

Polycrystalline-Si(poly-Si) thin-film transistors (TFTs) are being extensively studied to realize such electronic systems as very-high-resolution liquid crystal displays, systems on glass, static-random-access memory cells[1] and intelligent power chips.[2] It is well known that grain boundaries in poly-Si films degrade the performance of TFT. For example, grain boundaries in the channel region of TFT generate potential barriers for carrier transport along the channel which reduces the on-state current, and they also generate junction leakage at the source and the drain which increases the off-state current.

One promising approach for fabricating high performance poly-Si TFTs is to fabricate entire device channel region within a single grain of poly-Si films. To realize these devices, grains must be formed at controlled position. In solid phase crystallization of amorphous Si, we have recently proposed metal imprint technology[3] to form large(~10μm) grains at desired position. We have also demonstrated that TFTs fabricated in Si single grains prepared by the metal imprint technology have superior performance to those fabricated on conventional-SPC poly-Si films.[4]

In this work, we reports CMOS circuits composed of single-grain TFTs fabricated using the metal imprint technology. It is shown that single-grain TFTs have high threshold controllability and that the CMOS ring oscillator fabricated with single-grain TFTs have higher performance than those fabricated with conventional-SPC poly-Si TFTs.

2 Metal imprint technology

Figure 1 shows process steps of the imprint method. An array of pyramidal tips was prepared at the surface of (100) oriented Si by anisotropic etching with an alkali solution. Tip surface was then covered with vacuum evaporated Ni. An amorphous Si film was deposited using UHV evaporation on a Si substrate having thermal-SiO_2 at the surface. The tip-array was faced down to the a-Si film and pressed at the pressure of about 0.15MPa. After removing the tip-array substrate, the a-Si film on SiO_2 was annealed for crystallization in an N_2 ambient.

Figure 2 shows a scanning electron microscope image of a Si film imprinted with the Ni-coated tip array and annealed at 590°C for 7 hours. Prior to observation, Si crystal grains were chemically delineated. We can clearly see that crystal grains appear only at the sites imprinted with the tips which were arrayed in a square lattice pattern. This result clearly demonstrates that, with the Ni imprint, nucleation takes place almost coincidentally at the imprinted sites. From the results of TEM observation, the vast majority of the grains induced by the Ni imprint were ⟨111⟩ oriented single crystal. Grains up to about 10μm in diameter can be grown using this method.

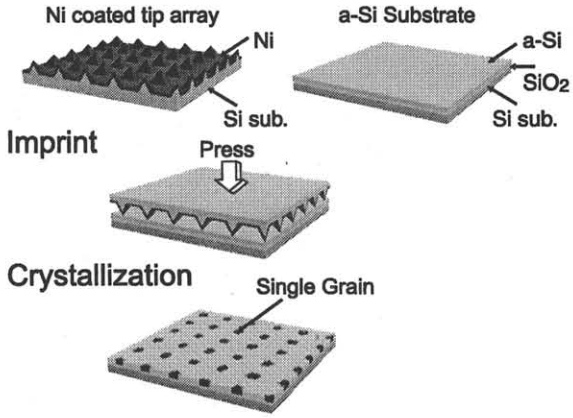

Fig. 1 Process sequence of the imprint technology. A tip-array is faced down and touched to the surface of an a-Si film. After removing the tip array, a-Si is annealed to crystallize.

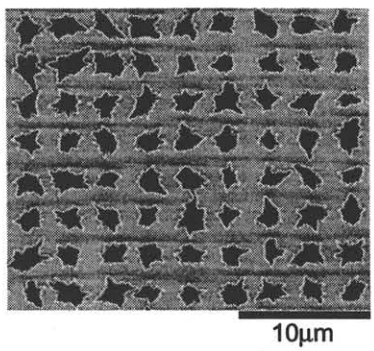

Fig. 2 SEM view of a Si film imprinted with a Ni-coated tip array and annealed at 590°C for 7 hours. The film was chemically delineated to remove a-Si region.

3 CMOS circuits with single-grain TFTs

In order to place the whole of TFT channel region within the large grain, the positions of imprinted grains and the positions of channels were aligned each other. To put it concretely, the position of Ni imprint point was aligned at source region of TFT in order to avoid contamination of the channel region with Ni. Crystallization was performed at 560°C in an N_2 ambient. After poly-Si films completely crystallized, high temperature annealing was applied at 1050°C for 10 hours for the purpose of reducing crystalline defects in grains. Al gate was used. Source/drain was formed by ion implantation. Gate oxide was formed using dry oxidation at 1050 °C and its thickness was 40 nm. The thickness of active layer was 80 nm. No plasma hydrogenation was performed to characterize intrinsic performance of TFTs. TFTs were also fabricated in the region of the same wafer where no imprint process was applied to characterize TFTs on conven-

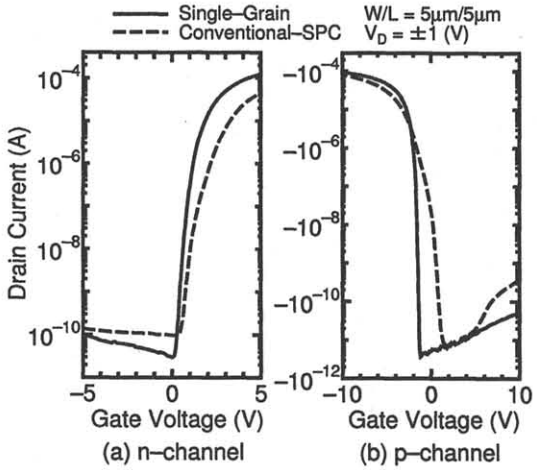

Fig. 3 Subthreshold characteristics of both (a) n–channel and (b) p–channel single–grain TFTs. Conventional–SPC TFTs are also shown.

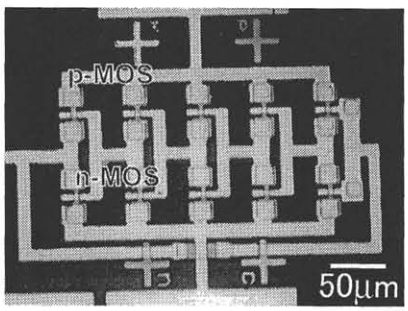

Fig. 4 Optical microscope view of a 5–stages CMOS ring oscillator.

tional SPC poly–Si.

Figure 3 shows subthreshold characteristic of n– and p–channel single–grain TFTs. Characteristics of conventional TFTs are also shown in the figure. We can see that the single–grain TFT shows superior transfer characteristic to the conventional–SPC poly–Si TFT. We did not observe any detrimental effect of the use of Ni. The single–grain TFT showed the field effect mobility up to about 450cm^2/Vs for n–channel and up to about 260cm^2/Vs for p–channel. Dispersion in mobility and in threshold voltage are about half for the single–grain TFT than for the conventional–SPC TFTs mobility.

Figure 4 shows an optical microscope view of the fabricated CMOS inverter. Both n– and p–channel TFTs were fabricated within single–grains prepared by metal imprint technology. Channel doping was carried out by implanting BF_2^+. It was possible to adjust the threshold voltages(V_{th}'s) of the single–grain TFTs to ±1V, while it was hard to adjust V_{th}'s of conventional–SPC TFTs within this range.

Transfer characteristic of the CMOS inverter fabricated with single–grain TFTs is shown in Figure 5. We can see that the CMOS inverter fabricated with single–grain TFT shows superior transfer characteristic to the inverter fabricated with conventional–SPC poly–Si TFT.

Figure 6 shows dependence of delay time on supply voltage of 5 stages ring oscillators. Gate width and length of TFT for these circuit were 3μm/3μm for n–channel and 3μm/5μm for p–channel. The CMOS inverter composed of Ni–imprint

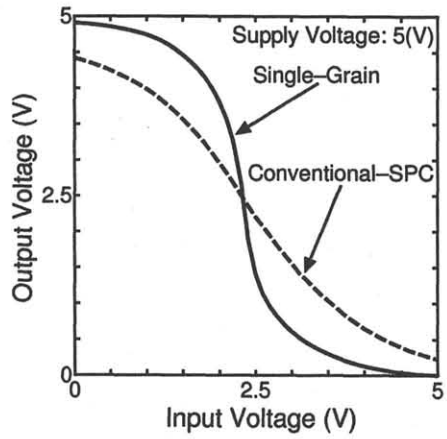

Fig. 5 Transfer characteristic of CMOS inverters fabricated with single–grain TFTs and with conventional–SPC TFTs.

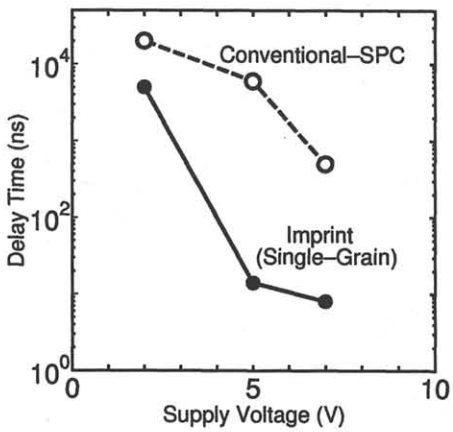

Fig. 6 Dependence of propagation delay time on supply voltage of 5-stages ring oscillator.

single–grain TFTs shows delay time smaller by two orders of magnitude than that composed of conventional–SPC TFTs. The propagation delay time of the single–grain TFT CMOS inverter is less than 8ns/stage at 7V.

4 Conclusions

In conclusion, the metal imprint technology is effective in preparing large–grain Si films. TFTs fabricated within the single–grain shows superior switching performance to the conventional–SPC TFT. This new technology offers high threshold voltage controllability of CMOS components and high dynamic performance of CMOS circuits.

Acknowledgments

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