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Characterization and Challenges of SOI Wafer Material at Present and its Perspective

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1. Introduction

SOI material is now established as the substrate of choice for advanced microprocessors applications, pushing SOI technology to ultrathin layers and high volume production. According to 2001 ITRS roadmap [1], one can see that 65nm and even 45nm are the critical defect size to be detected when meeting the 90nm node for defect monitoring. This paper deals with SOI characterization techniques and focusses on the challenges encountered with SOI structures in terms of defectivity monitoring. SOI technologies availability regarding quality and volume production will be discussed, with a focus on Unibond SOI roadmap.

2. SOI wafers characterization

Fig. 1 is describing key properties of an SOI wafer and most of the defects that could occur on these wafers. In a production environment, main parameters are checked through physical, chemical and electrical characterization techniques. Table I is showing typical test flow used for wafer quality screening in Unibond® manufacturing line. Performance and requirements encountered for each monitoring step will be discussed. Most of the techniques involved are standard in semiconductor industry such as for example, reflectometry or ellipsometry for film thicknesses, AFM for surface roughness, or laser scattering for defectivity. However, major adaptation or dedicated revelation have to be involved to fit with SOI properties, such as HF defects revelation technique.

Film thickness measurement is made using ellipsometry or reflectometry techniques. For wafer bonding based SOI technologies, insulating layer (BOX) is first grown and then embedded in the structure. Then, silicon layer and oxide layer can be measured separately, allowing accurate monitoring by reflectometry. For Simox technique, surface and interface roughness combined with BOX being generated in the silicon volume requires more complex models with ellipsometry technique for accurate layer thickness monitoring.

Using laser scattering inspection systems for defect detection on silicon wafers , the major limitation for low threshold operation is surface roughness, which increases the background noise measured from the wafer[2]. This background scattering signal generated by the micro-roughness is often called haze. It has been demonstrated in the case of SOI wafers that reflectivity is an additional contributor to wafer noise [3]. Fig. 2 shows reflectivity as a function of silicon and oxide thicknesses. Such reflectivity changes could lead to threshold limitations during inspection from 100nm to 200nm for SOI wafers showing surface properties equivalent to bulk silicon (sizing based on Latex Sphere Equivalent (LSE) standards over a constant substrate reflectivity model) [3]. Reflectivity also impacts sizing accuracy on the wafer inducing correlation between size and thickness uniformity.

3. SOI wafers challenges

When reviewing ITRS roadmap targets, several challenging items appear. Silicon film thickness and uniformity are the most aggressive, with values typically of 10nm and ± 5%, 6σ. These requirements, leads to 10Å thickness accuracy on a 300mm wafer. This represents both manufacturing and metrology challenges that will be discussed. All SOI technologies have to be improved in order to close gap between current performance and 2004 objectives. As a general trend, it appears that such high uniformity needs to be guaranteed whatever the spatial wavelength of the measurement down to Å scale what is currently the domain of roughness measurement, . The "nano-uniformity " will certainly be the key challenge rising metrology difficulty.

In order to scale existing Unibond® strategy to ultra thin new 300mm Unibond® products have been developped. Uniformity results are shown for a 200 Å silicon layer, exhibiting a ± 20Å uniformity, all wafers all sites, using a 3mm edge exclusion (Fig.3). Then, outstanding performance are achieved both in terms of wafer-to-wafer and on-wafer uniformities, demonstrating no showstopper for Smart-Cut® technology when talking about ultra thin film SOI (Fig. 4). While taking benefits from 200 mm volume production maturity, all other SOI structure properties such as defectivity, surface and interface quality, metallic and organic contamination levels are proving the same high level of quality than 200mm Unibond®. Process optimization are now involved in order to further improve uniformity for film thicknesses down to 100 Å.

In addition defectivity monitoring needs to be improved for 65nm node, requiring thresholds lower than 50nm detection on thin SOI films.

4. SOI perspective: The Smart-Cut® example

In the continuous search for increased device operating speed, SOI film is scaled down to nm level. Further generation are already announced involving strain silicon and/or SiGe in so-called SSOI and SGOI structures. SOI technologies needs to be compatible with these future

options in order to demonstrate extendability to future device generations.

Smart-Cut® transfer has been achieved in numerous III-IV compounds and especially in SiGe, demonstrating its flexibility and its ability to enable new solutions.

5. Conclusion

Characterization technqiues have been developped or adapted to SOI material. These techniques are compatible with high volume production and able to guaranty control levels required for device production. While scaling down film thickness, layer uniformity is the most important challenge for both manufacturing and metrology. Several SOI technologies are showing promising improvements but needs to be compatible with engineered top layers required for sub 90nm device generation.

References :

[1] http://public.itrs.net

[2] KLA-Tencor Surfscan SP1 Application note, Recipe Guideline for the SP1-TBI, Aug 00, Andrew Zeng et al.

[3] C.Maleville et al., 2000 SOI conference, p.19.

Table I : Characterization flow in Unibond® production.

Parameter	Technique	Comment
Layers thicknesses	Full wafer reflectometry	Oxide and silicon monitoring
Macroscopic defects	Visual inspection	Voids, Large scratches, edge inspection,...
Microscopic defects	Laser scattering tools	Light Point Defects and Large Area Defects, Scratches,...
Silicon layer threading defects	HF revelation + decorated defects counting	SP1 full wafer detection for low detection limit. One wafer per batch
Cristalline defects	Secco revelation	Microscope counting on samples
Metallic contamination	VPD ICPMS	Front and back face analysis.
Electrical parameters	Pseudo-MOS measurements	Mobility and interface state density

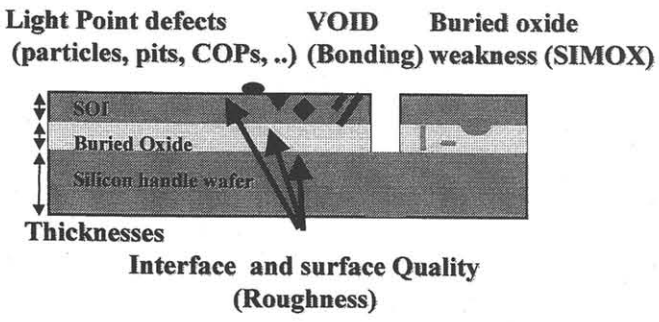

Fig 1 Typical defects and parameters to be monitored for an SOI structure.

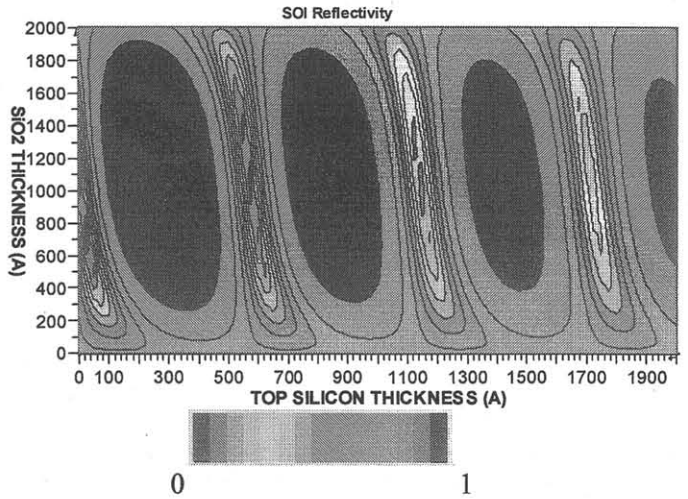

Fig.2 : 2D reflectivity curves showing oxide and silicon thicknesses influence on reflectivity.

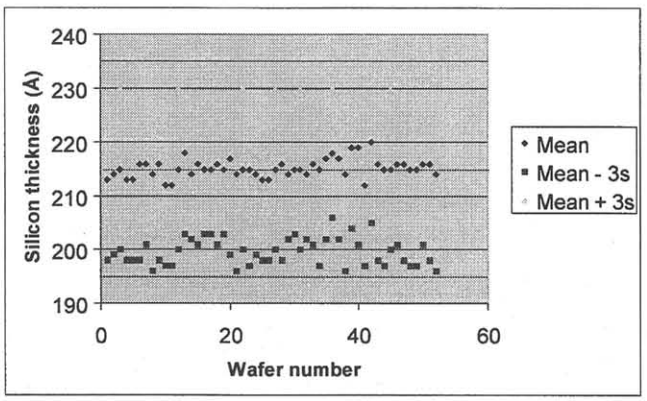

Fig. 3 : 300mm Unibond® silicon thickness. 215/1450Å structures verifying ±20Å, all wafers, all sites.

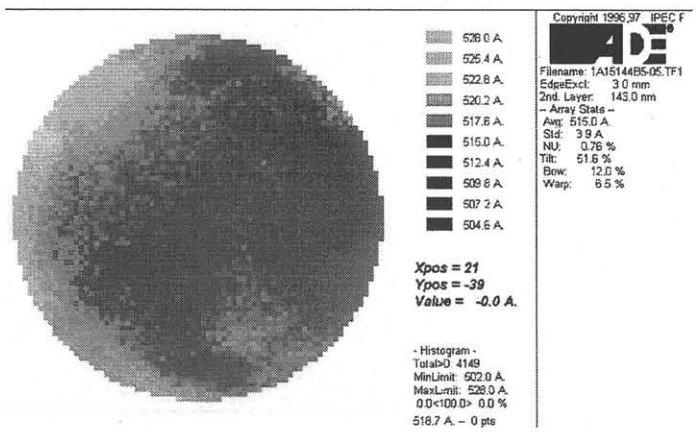

Fig. 4: 300mm Unibond® thickness map for a 500/1500 Å structure – 3mm edge exclusion. More than 4000 points measured, σ<4Å and Range <25Å