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Reduction of Pattern-Edge Defects in Partial SOI by LII (Light-Ion Implantation) Technique

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Abstract

We demonstrated the reduction of pattern-edge defects in partial SOI by using the light-ion implantation (LII) technique. Compared to the conventional SIMOX, the LII process causes less damage and can therefore reduce the defect density at the pattern edge in partial SOI structures. An SON formed by LII process showed a further reduction of the defect density, probably because the stress induced by the SiO₂ formation can be minimized, and its surface was extremely flat. Therefore, the LII has great advantages for fabricating partial SOI as a substrate for SOC.

1. Introduction

Partial SOI is attractive for the use as a superior substrate for Si on chip (SOC), because it can simultaneously provide both a high-speed logic circuit on the SOI region and high-performance DRAM cells on the bulk region. So far, patterned SIMOX, in which O⁺ ions are implanted through a patterned mask, has usually been used for partial SOI fabrication [1]. However, the substrates fabricated by patterned SIMOX usually contain a high defect density especially at the boundaries between the SOI and the non-SOI region.

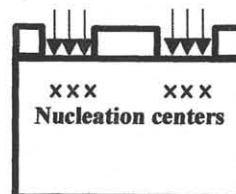
We have demonstrated a new SOI formation technique in which O⁺ implantation is eliminated from the SIMOX process by applying light-ion implantation and annealing appropriately using atmospheric oxygen to enhance the oxygen precipitation at the implantation damage (LII technique) [2]. The LII causes less damage than SIMOX and can therefore provide a better crystalline quality, because the implantation damage is much less than in the conventional SIMOX. In this study, we applied the LII technique to obtain a partial SOI substrate and then evaluated the fabricated structures.

2. Experiment

Figure 1 shows the partial SOI fabrication process using the LII technique. In this process, light ions are partially implanted into the Si substrate to create the

nucleation centers for the oxygen precipitation [Fig. 1(a)]. The sample is then annealed in the Ar/O₂ atmosphere to enhance the oxygen precipitation. The precipitates also grow and coalesce during the annealing [Fig. 1(b)]. A partial SOI structure appears after the annealing. In the present study, we implanted He⁺ as light ions through a 0.5- μ m-thick patterned SiO₂ mask at a 45-KeV acceleration voltage and in $3.5 - 4 \times 10^{17}/\text{cm}^2$ doses. Then, the samples were annealed at 1340°C for four hours in an Ar/O₂ atmosphere at a ramping rate of 0.02 to 1°C/min from 1200 to 1340°C and at an Ar/O₂ ratio of 100/1-20. The fabricated structures were evaluated by SEM and

(1) Light ion implantation



(2) Anneal (Ar/O₂)



(3) Partial SOI formation

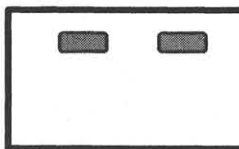


Fig. 1 Partial SOI fabrication by LII.
TEM.

3. Results and discussion

We believe the LII technique causes less damage to Si crystals and therefore fewer defects in SOI compared with conventional SIMOX. Especially for the partial SOI formation, highly defective areas at the boundaries

between SOI and non-SOI regions have been a severe problem. Therefore, we thought that a partial SOI formation would demonstrate LII's high potential. Figure 2 shows the TEM image of the partial SOI formed by LII technique. The substrate surface was not completely flat, because the SOI layer was thicker at the pattern edge than that at the pattern center [Fig. 2(a)]. Some defects were also observed at the pattern edge [Fig. 2 (b)]. However, both the quality of the surface flatness and that of the defect density may be better than those produced by patterned SIMOX.

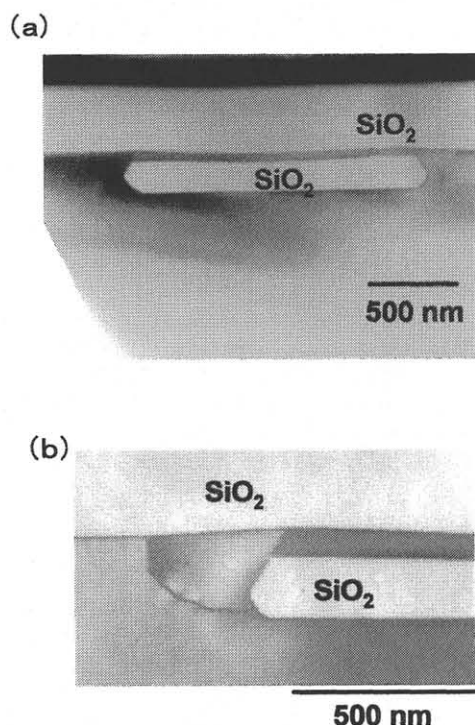


Fig. 2 Partial SOI formed by LII

By changing the annealing conditions, we could control the ratio of the volume filled by SiO_2 in the insulating layer. An SOI structure with a small SiO_2 volume in the insulating layer may be called Si-on-nothing (SON) rather than SOI. An SON is usually fabricated by high-aspect trench formation and high-temperature annealing in an H_2 ambient or by preferential etching of a sacrificial layer [3]. The advantages of the LII technique are its simple fabrication process and the possibility of coating the inner surface of the buried empty space with SiO_2 . The defects in an SON formed by LII may also be further reduced, because stress caused by the volume expansion due to the SiO_2 formation should not be significant.

Figure 3 shows the SON fabricated by LII. The SON surface was extremely flat compared with the partial SOI and SON surfaces fabricated by other techniques, although the thickness of the insulating layer was not completely uniform [Fig. 3(a)]. This flat surface would be a great advantage for an ULSI-SOC, because state-of-the-art photolithography requires an extremely flat surface due to a focal depth limitation. Furthermore, no defects were observed, even at the pattern edge [Fig. 3(b)]. The stress induced by the buried SiO_2 formation might have been minimized when the insulating layer was replaced by a vacancy from the SiO_2 , and therefore the pattern-edge defects disappeared. The inner surface of the buried vacancy was covered by SiO_2 film. This is expected to provide good interface electrical properties. The SiO_2 film was thicker at the sidewall than at the top and bottom.

Acknowledgements

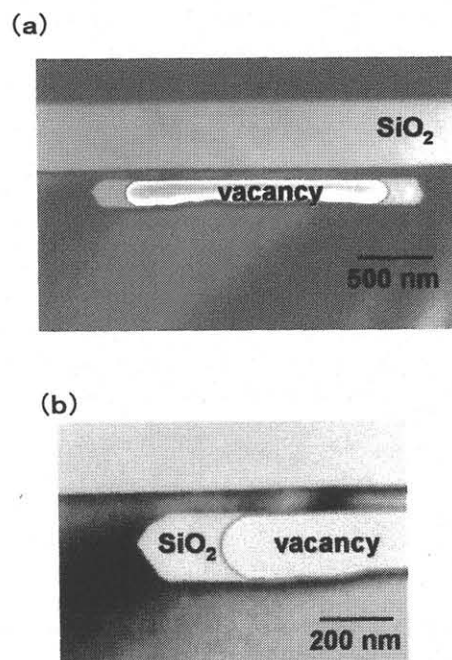


Fig. 3 SON formed by LII

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