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Effective Metal Gettering Technique using Polysilicon Substrate Contact Structure for SOI Devices

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1. Introduction

Thin-film silicon-on-insulator (SOI) is attractive as the key technology for low-voltage, low-power and high-speed operation of semiconductor devices. We have proposed device structures with the partial trench isolation and the hybrid trench isolation, and have reported their validity [1], [2]. Intensive efforts have been made to improve wafer qualities, and hence these have made remarkable progress.

However, it is supposed that device characteristics on SOI wafers tend to be strongly influenced by metal contamination compared with that on bulk wafers, because of the buried oxide (BOX) layer. Figure 1 shows the behavior of metal contaminants on bulk and SOI wafers, schematically. Most of metal contaminants on bulk wafers are captured by extrinsic gettering layer such as polysilicon back coating and/or intrinsic gettering site such as oxygen precipitates during high temperature annealing in device fabrication processes. It is well known that the BOX layer suppresses diffusion of some metal contaminants into the support substrate from the SOI layer and that the contaminants are remained in the SOI layer [3], and metal-silicon compounds will be formed. These compounds become a cause of degradation of device characteristics, such as anomalous junction leakage currents and the lack of GOI. Higher performance and reliable devices may require lower metal contamination level. It is considered that gettering techniques by gettering sites contiguous with the SOI layer are necessary in order to improve SOI device characteristics and yield by avoiding metal contamination in the near future.

In this paper, we propose an effective gettering technique using a polysilicon substrate contact structure contiguous with the SOI layer. Moreover, we also propose an SOI device structure that has gettering ability without losing advantages of the SOI structure.

2. Sample Preparation

P-type (100) oriented 200 mm ϕ bonded SOI wafers with 200nm SOI and 400 nm BOX were used. The SOI thickness was reduced into 150 nm by thermal oxidation and HF removal. The sample structure in this experiment is shown in Fig. 2. Polysilicon plugs connect the SOI layer to the support substrate. The plugs are made of phosphorus-doped polysilicon. We also prepared another sample with the SOI layer into which BF_2 was implanted with the dose of $4\text{E}15$ ions/ cm^2 in order to evaluate the gettering ability of polysilicon plugs at the area that has ion-implantation induced defects. The samples were intentionally contaminated with Co atoms and annealed at 850°C for 30 seconds in nitrogen atmosphere.

3. Evaluation Method of the Gettering Ability

We evaluated the gettering ability of polysilicon plugs by measuring the density and distribution of Co induced defects at the area close to polysilicon plugs. Schematic images of a formation mechanism of the defect are shown in Fig. 3. The defects are formed by the heat treatment following intentional Co contamination in the SOI layer. Figure 4 shows a cross-sectional TEM photograph and a result of TEM-EELS analysis of the defect. From these results, it is found that the defects are introduced parallel to Si (111)

plane and a part of the defect reaches the SOI/BOX interface. Therefore, it is considered the defect is a Co silicide platelet [4]. Figure 5 is the cross-sectional SEM photograph of the defect after HF dipping, which corresponded to Fig. 3 (C). The BOX layer under the defect was etched with HF solution. It is found that the Co induced defect become the origin of HF defect. Therefore, Co induced defects can be delineated as HF defects as shown in Fig. 6 and the density of Co induced defects can be evaluated as the HF defect density.

In this study, the evaluation of density and distribution of Co induced defects was carried out in this way.

4. Gettering Ability of Poly-Si Plug

An optical image of Co induced defects after HF dipping in the BF_2 -implanted sample is shown in Fig. 7. The defects are not generated near the plugs. Figure 8 shows the dependence of the defect density on the distance from polysilicon plug area. It is found that a width of non-defective area in non-implanted sample is wider than that in the BF_2 -implanted sample. No defects are generated in non-implanted sample. On the other hand, the width of non-defective area is about 10 μm in the BF_2 -implanted sample. It is clarified that polysilicon plugs have the ability to decrease metal contaminants in quantity from high implanted dose area, such as source and drain region.

It was reported that diffusivity of Co in Si was large [4], and it is expected that the diffusion length will be over 100 μm on this heat treatment condition. Every point is in the distance of less than 45 μm from plugs in this study. Therefore, it is considered that Co contaminants were gettered and no defects were generated in non-implanted sample. In the case of the BF_2 -implanted sample, it is considered that crystal defects induced during ion implantation work as gettering sites and Co contaminants are gettered by these defects. Therefore non-defective area may become smaller than that in non-implanted sample.

Figure 9 shows a result of the defect observation at the BF_2 -implanted area with high-density plugs. The largest distance between adjoining polysilicon plugs is 5 μm . It is confirmed that no defects are generated at this area.

5. SOI Device Structure with Gettering Ability

A schematic image of an SOI device structure that has metal gettering ability is shown in Fig. 10. Polysilicon plugs connect the SOI layer under the partial trench isolation to the support substrate. This gettering technique is valid for devices with partial trench isolation because the silicon layer under the isolation connects adjacent active area. Therefore, it is expected that the devices with partial trench isolation have still higher reliability by using this gettering technique. Moreover, this structure can add the metal gettering ability to SOI devices, without losing the advantage of the SOI structure.

6. Conclusions

The gettering ability of polysilicon plugs that connect the SOI layer to the support substrate is evaluated by focusing the density of

Co induced defects. It is confirmed that no defects are generated at the area from polysilicon plug area to distance of 45 μm in non-implanted sample, and 10 μm in the BF_2 -implanted sample. Therefore, the effect of gettering can be expected enough in real devices.

References
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 [3] J. Furihata, et al., Jpn. J. Appl. Phys. Vol. 39, p. 2251, 2000.
 [4] K. Graff "Metal Impurities in Silicon-Device Fabrication", Springer, Berlin, 2000.

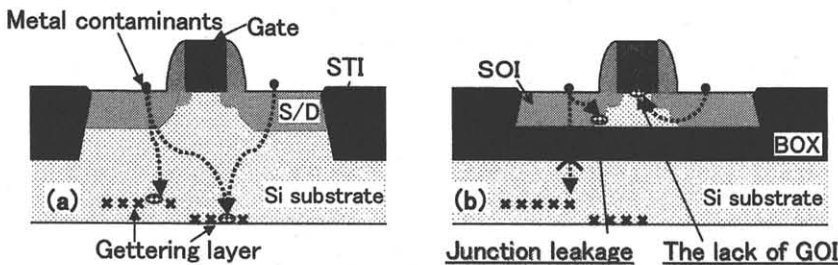


Fig.1 Schematic images of the behavior of metal impurities on (a) bulk and (b) SOI wafers.

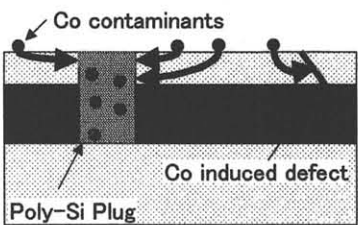


Fig.2 Sample structure in this experiment. Polysilicon plugs connect the SOI layer to the support substrate.

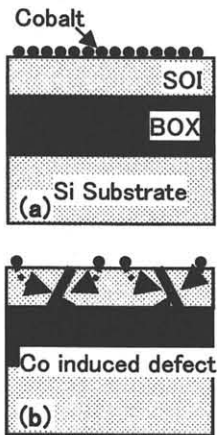


Fig.3 Schematic images of a formation mechanism of Co induced defects.
 (a) Intentional Co contamination
 (b) Co induced defects formation by the heat treatment
 (c) HF defects formation by HF dipping

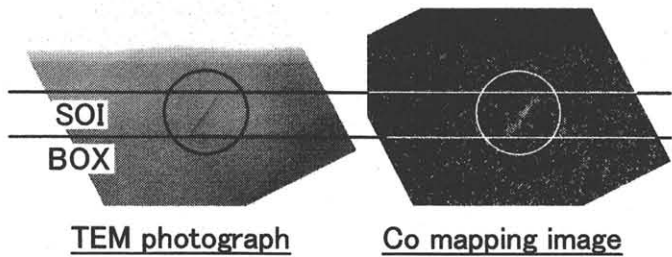


Fig.4 Cross-sectional TEM photograph and a result of TEM-EELS analysis of a Co induced defect.

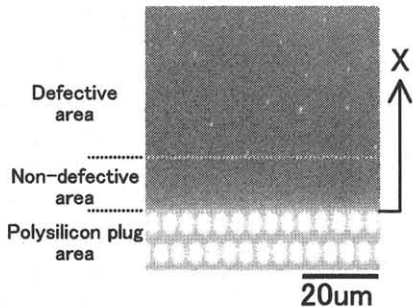


Fig.7 Optical view of Co induced defects in the BF_2 -implanted sample.

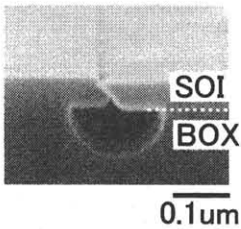


Fig.5 Cross sectional SEM photograph of a Co induced defect after HF dipping.

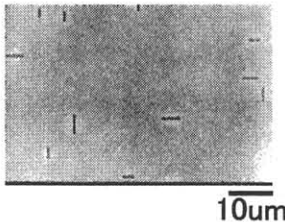


Fig.6 Top view of Co induced defects by SEM.

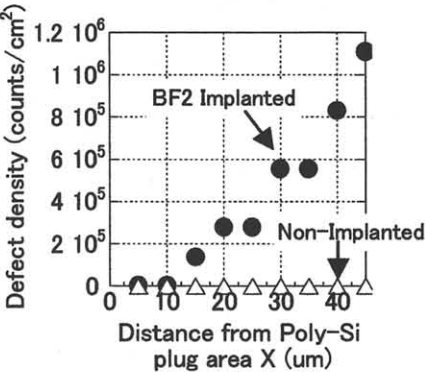


Fig.8 Dependence of the defect density on the distance from the polysilicon plug area.
 (●: BF_2 -implanted, \triangle : non-implant)

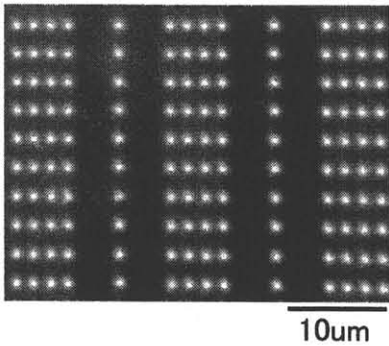


Fig.9 Optical view at the BF_2 -implanted area with high-density plugs.

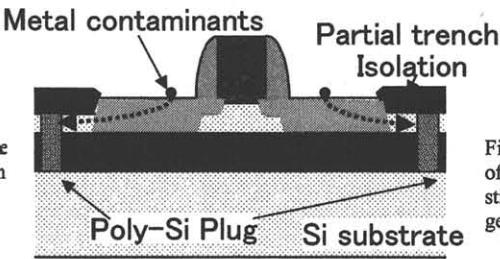


Fig.10 Schematic image of an SOI device structure that has metal gettering ability.