Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 794-795

D-8-4

Silicon-On-Low-K Substrate(SOLK) Technology for High-Speed and Low-Power Devices

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1. Introduction

Signal propagation delay and cross talk caused by the metal wiring are the most crucial problem in current LSIs. Therefore, a multilevel metallization technology using copper as metal wiring and low-k material as interlayer dielectric has been developed in order to mitigate such wiring related problem by reducing the wiring resistance and wiring capacitance. However, signal propagation delay and cross talk caused by the silicon substrate also become crucial as the clock frequency increases beyond several GHz. It is also problem that more energy is consumed by the lossy silicon substrate during the signal propagation. Then, we employ a low-k substrate instead of the silicon substrate to solve the substrate related problems. Of course, the crystalline silicon is used as the transistor channel.

We call this technology using a low-k substrate Silicon-On-Low-K substrate (SOLK)

2. SOLK Technology

Figure 1 shows the cross-sectional structure of the SOLK MOSFET. In SOLK technology, the LSI wafer with fully depleted SOI MOSFETs is face-down bonded onto a low-k substrate with the metal electrode on the backside. The silicon substrate of SOI wafer is completely removed to expose the buried oxide (BOX) and metal wirings are formed on the BOX. Thus, we can eliminate the substrate loss and dramatically reduce the stray capacitances between MOSFET or metal wiring and the substrate.

3. Fabrication and Evaluation of SOLK Devices

So far, we have fabricated various kinds of 3D LSIs using our new wafer stacking technique [1]-[5]. Then, we apply this wafer stacking technique to fabricate SOLK MOSFET. The fabrication process sequence of SOLK MOSFET is shown in Fig.2. First of all, we fabricated FD-SOI MOSFET. Device wafer with SOI film thickness of 50nm and buried oxide thickness of 500nm was used as the starting wafer (Fig. 2(a)). After the fabrication of FD-SOI MOSFET, many steps with the step height of several μm exist on the top surface. In order to achieve a successful wafer bonding on the low-k substrate, we have to minimize the surface steps and obtain the extremely flat surface. Then, in order to obtain the flat surface, we deposited the TEOS-SiO_2 on the surface of the SOI device wafer and planarized the surface using the chemical-mechanical polishing (CMP) method (Fig. 2(b)). Figure 3 shows the photomicrographs of the SOI device wafers after wafer bonding onto the quartz glass with and without the surface planarization. Low-k material was also used as the adhesive material (glue material) to bond the wafer onto the low-k layer on the quartz glass. Fig. 3(a) shows the result for the wafer without the surface planarization and hence with the step height of around 1 μm. It is clear in the figure that there are many voids and the SOI wafer was bonded to the low-k layer on the quartz glass only in the limited area. On the other hand, the perfect bonding between SOI and low-k layer were achieved as shown in Fig. 3(b) when the step height in the surface was reduced to less than 40nm by CMP. In the wafer bonding with the planarization procedure, low-k glue layer was formed on the SOI device wafer after planarizing the surface. Polyimide or Benzocyclobutene (BCB) is used as a low-k material compatible with CMOS process and is stable at the processing temperature up to 400℃. Both polyimide and BCB can be also used as a glue layer. After the formation of low-k layer, the SOI wafer was face-down bonded onto the quartz glass with the low-k glue layer on the surface (Fig.2(c)). Then, we removed the silicon substrate to expose the buried oxide (Fig.2(d)). RIE with SF_6 gas was used to remove the silicon substrate. The buried oxide was used as a silicon etch stop. After the formation of contact via through the buried oxide and the back metallization, we can obtain the SOLK MOSFET (Fig.2(e)).

The photograph of SOLK device chips fabricated according the process sequence described above is shown in Fig.4. As is obvious in the figure, the fabricated SOLK device chip was completely transparent to the visible light since a quartz glass with the low-k layer was used as the low-k substrate.

4. Results and Discussions

Figure 5 shows the SEM cross sectional view of the fabricated SOLK MOSFET. It is clearly seen in the figure that the SOI wafer is face-down bonded onto the quartz glass and the silicon substrate of the SOI wafer is completely removed.

Figure 6 shows the subthreshold characteristics of FD-SOLK MOSFET and FD-SOI MOSFET. The characteristic for FD-SOI MOSFET was the same as that measured before the SOLK process. The excellent subthreshold characteristics were obtained even after the SOLK process.

5. Conclusion

We proposed a new Silicon-On-Low-K substrate (SOLK) technology to achieve a high speed and low power devices by eliminating the substrate loss and reducing the stray capacitances using a low-k substrate instead of the silicon substrate. We succeeded to fabricate SOLK MOSFET with transparent low-k substrate. We obtained the excellent subthreshold characteristics in SOLK MOSFET even after the SOLK process.

References

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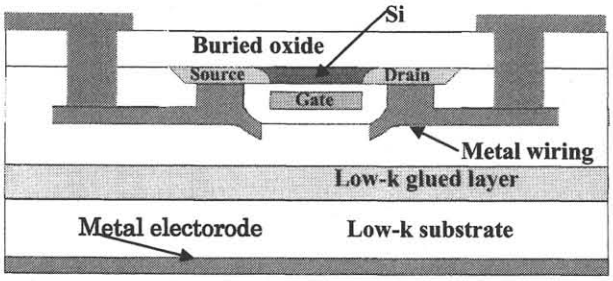


Fig.1 Cross-sectional structure of SOLK

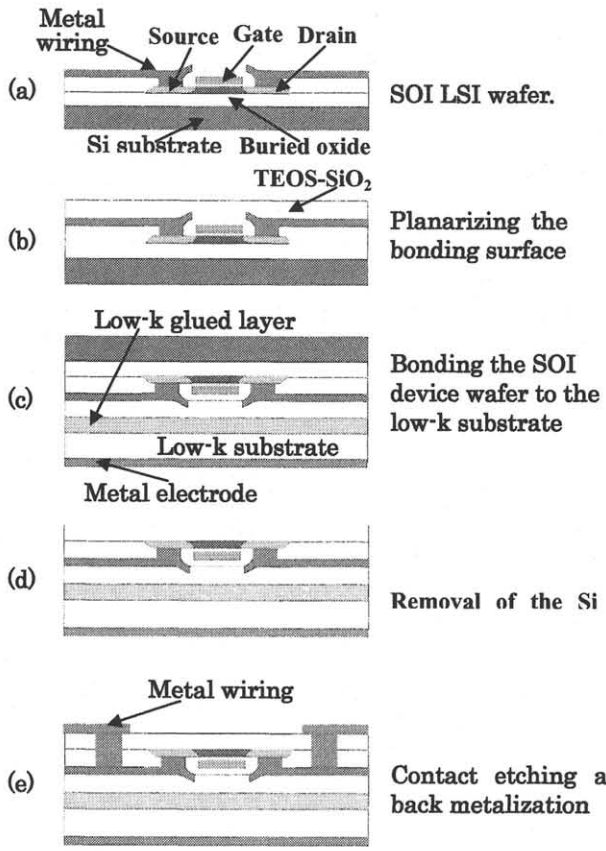
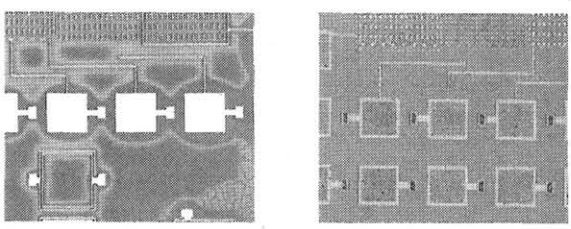


Fig.2 Fabrication process flow.



(a) Before Planarization (b) After Planarization

Fig.3 Bonding results with different surface roughness.

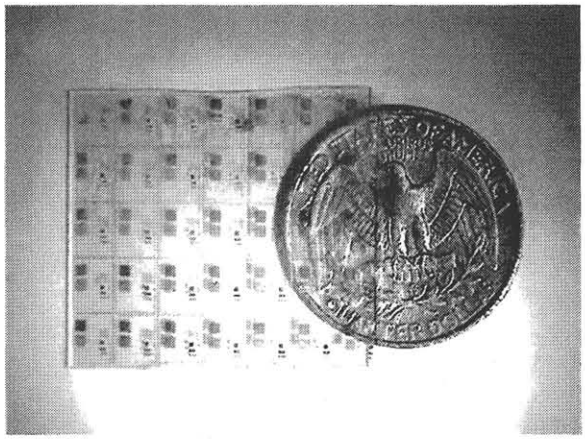


Fig.4 Transparent SOLK chip with quartz substrate.

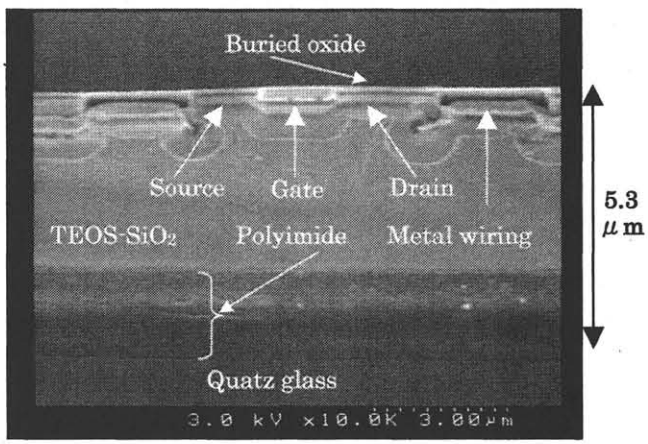


Fig.5 SEM cross-sectional view of SOLK MOSFET.

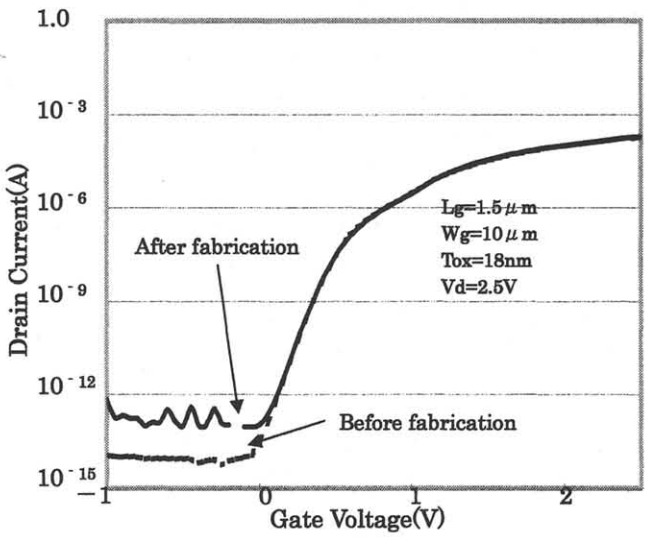


Fig.6 Subthreshould characteristics of FD-SOLK MOSFET and FD-SOI MOSFET