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Dynamic Floating Body Effects in Fully Depleted SOI MOSFET's

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1.Abstract

By using high-frequency Ring Oscillators, the dynamic Floating Body Effect(FBE) and delay time on fully depleted Silicon-on-insulator(FD-SOI) CMOS inverters have been evaluated, for the first time, up to 500 MHz. As a result of dynamic FBE, an increase of inverter delay time is observed for frequencies above 150 MHz for the 0.25um and 0.35um FD-SOI evaluated devices.

2. Introduction

SOI devices are recently notable for low-power portable terminal applications. As traditional study, characteristics of FD-SOI are as follows. Steep subthreshold[1], Kinkless[2], Enhancement of current driver-ability[3],[4], Stability for floating body effects[5],[6] However the body potential of FD-SOI is not fixed because of device structure. Therefore FD-SOI characteristics fluctuate by the body potential variation. In this paper, we describe the delay characteristics for dynamic FBE by evaluating the ring-oscillator circuits fabricated by 0.25um and 0.35um FD-SOI technologies. From the analysis of delay characteristics, the delay time instability is caused by the dynamic body potential variation owing to the unbalance of charging of floating body by impact ionization and discharge of diode currents.

3. Experiment

The dynamic floating body effects are evaluated by measuring the propagation delay time(Tpd) for various CMOS inverter-type ring-oscillators with different number of stages(N).[fro=1/2NTpd, with N=11,23,37,47,79,101] The measured circuits which include a 256-divider due to be measurable high-frequency is shown in Fig. 1. Brief transistor description and characteristics to demonstrate the transistors are really FD are shown in Table 1 and Fig. 2., respectively.

4. Results and Discussion

Dependence of delay on oscillating frequency

The dependence of delay time on oscillating frequency is shown in Fig. 3 at Vdd=1V. When the oscillating frequency is over 150 MHz, the propagation delay time increases with increase of oscillating frequency. The Maximum increase rate is 9.6% at 481 MHz and room temperature. The above phenomenon in PD-SOI has been observed, and it is caused by the majority carrier re-distribution effect[7]. However this majority carrier re-distribution effect does not occur in FD-SOI, since the body is usually depleted.

Influence of fixed body potential

The influence of fixed body potential is shown in Fig. 4. To fix the body potential, H-gate body-tied transistors are used in consideration of carrier capturing ability. As shown in Figure, when the body potential is fixed, the dependence of delay time on oscillating frequency is not observed.

Study on factor of body potential variation

The drain voltage affects the transistor body potential and the accumulation of majority carriers generated by impact ionization and thermal generation. In DC conditions, this effect can be evaluated by the Vth lowering enhancement with Vds[8] as shown in Fig. 5. For the 0.35um FD-SOI devices, impact ionization enhances majority carrier accumulation in the body for Vds >Vdk(1.3V).

Influence of body potential variation on delay time

The delay time fluctuation for a change of supply voltage which means the difference of impact ionization is evaluated. That result is shown in Fig. 6. For the 0.35um FD-SOI devices, when supply voltage is 0.8V, increasing delay time is observed in whole frequency. On the other hand, when supply voltage is 1.8V, increasing delay time is observed over 150 MHz. The maximum rate of increase is 4.8%, and it is less than 8.1% when a supply voltage is 0.8V. Fig. 7 shows the dependence of frequency of delay time increased by 5% on supply voltage. Fig. 8 shows the dependence of dynamic Vth extracted from RC time constant on oscillating frequency. Thus the delay time fluctuation is dependent on the supply voltage, and it is caused by the dynamic body potential variation observed as dynamic Vth variation.

Mechanism of delay time fluctuation

Using the CMOS inverter IN, OUT and body potential transition and the equivalent circuit shown in Fig. 9. and 10, respectively, the mechanism of delay time fluctuation is explained by corresponding region number in Fig. 9 for the NMOS transistor.

1), 3) Body potential is affected by capacitive coupling with gate and drain.

2) Body potential is almost at equilibrium because of no impact-ionization.

4) Body potential is determined by the balance of accumulated majority carriers, generated by impact-ionization and thermal generation, and disappeared carriers through body-source diode current. The accumulated majority carriers are dependent on supply voltage. Moreover this balance is dependent on frequency, because the body potential can be gotten to steady state in

low frequency region, not in high frequency region.

Fig. 11 compares the TCAD simulated waveforms at f=100 MHz and f=500MHz for the FD-SOI CMOS inverters. The delay time of the falling output, which is determined by the NMOS transistor drive ability, and hence its Vth, is affected by the body potential Vbs before this transition[4 in Fig.9]. TCAD simulations confirm that at f=500MHz, the body potential Vbs is lower than at f=100MHz, resulting in higher dynamic Vth(Fig.8) and reduced driving current.

5. Conclusions

For the first time, the FBE in FD-SOI transistor has been evaluated up to 500 MHz. The propagation delay time is dependent on the frequency and supply voltage owing to dynamic body potential variation. These results suggest that dynamic FBE need to be accounted for in the design and modeling of FD-SOI.

Acknowledgments

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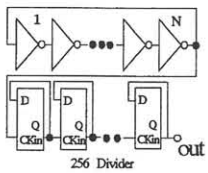

Fig. 1 Measurement Circuit

Table 1. Transistor Description

	0.25um Technology	0.35um Technology
Tox[nm]	3.5	7
Tsi[nm]	50	50
Tbox[nm]	115	110
Vth_n[V] (@W=10um,Triode)	0.12	0.13

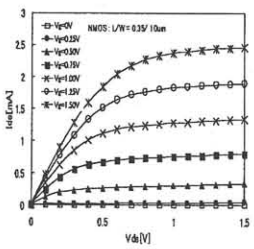

Fig. 2 Kink-free Characteristic of 0.35um FD-SOI transistor

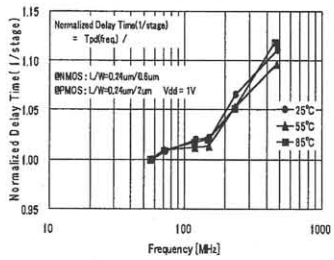

Fig. 3 Dependence of delay time variation on frequency for the L=0.24um FD-SOI with floating body transistor at Vdd=1V

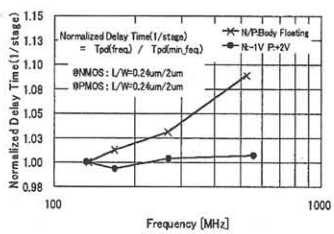

Fig. 4 Influence of fixed body potential to delay time variation

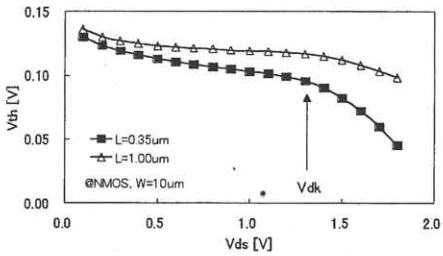

Fig. 5 Threshold voltage characteristics for drain voltage

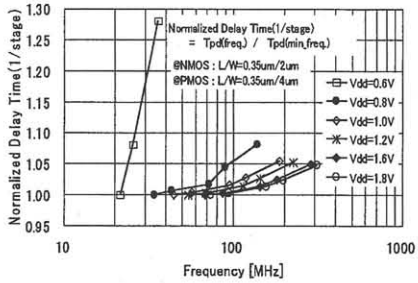

Fig. 6 Dependence of delay time variation on frequency and supply voltage for the L=0.35um FD-SOI

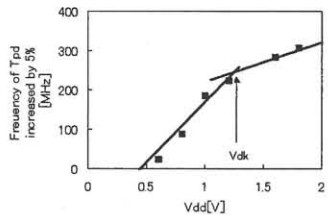

Fig. 7 Dependence of frequency of Tpd increased by 5% on Vdd for the L=0.35um FD-SOI

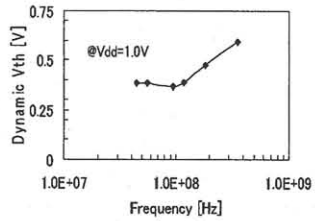

Fig. 8 Dependence of dynamic Vth on frequency

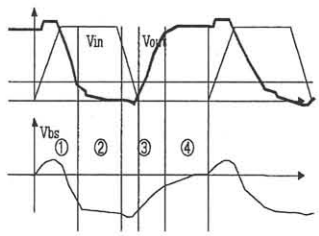

Fig. 9 IN, OUT and body potential transition for NMOS

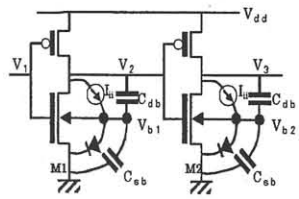

Fig. 10 equivalent circuit for Inverter

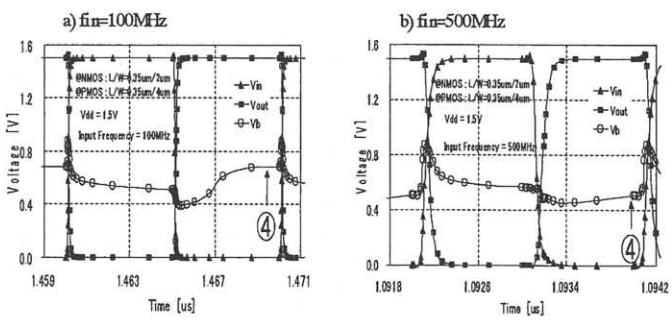

Fig. 11 Verification of delay time fluctuation mechanism using TCAD simulation ;Vthn=0.13V and Vdd=1.5V