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FD-SOI MOSFET with Self-Aligned Gate Formed on Recessed Channel

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1. Introduction

Owing to their sharp sub-threshold slope characteristics, Fully-Depleted SOI MOSFET's are strong candidate for low power and/or high-speed IC applications. To get fully depleted (FD) performance in scaled down SOI MOSFET, SOI layer has to be thinner. For example, in sub-0.1μm generation, it is predicted that a 20nm thick SOI layer will be required [1].

In conventional process, the thickness of whole SOI layer on the wafer is decided at the beginning of the fabrication flow, and the resulting thickness of the source/drain regions is the same as the channel region. Thinner SOI results in higher parasitic source/drain resistance, which reduces the drive current of MOSFET.

For the reduction of parasitic resistance, raised source/drain technology, with selective epitaxial growth (SEG) of Si and salicide, has been proposed. However, SEG process has several problems. Facet formation influence scale-down of devices. SEG technology needs to remove native oxide completely just before deposition. In-situ H_2 bake treatment is important for getting pure surface of Si. But this treatment involves highly thermal budget.

The SOI MOSFET with recessed channel structure has also been described [2]. In that report, however, gate formation needs alignment margin for recessed area. As a result, the MOSFET's area is larger, and then, results in an asymmetrical MOSFET due the misalignment between the gate electrode and the recess area edge that may degrade the LSI performance.

A process which has self-aligned gate process on recessed channel by using LOCOS technology has been reported in [3]. The resulting gate electrode edge has bird's beak shape, this structure can't apply to salicide process, which needs sidewall spacer.

In this paper, we propose the way to form FD-SOI MOSFET with self-aligned gate on recessed channel. We report the device structure, fabrication sequence and device characteristics.

2. Experiment

Fig.1 schematically shows the process steps of the new SOI MOSFET fabrication. After formation of isolation area, pad oxide and nitride film are formed. By using photolithography and dry etching, the SiN_x film on channel area is removed as shown in Fig. 1 (a). Then for control of channel thickness, local oxidation is performed as shown in Fig. 1 (b). After removing the local oxide, pad oxide on channel area and CVD SiN_x film are formed, and sidewall spacers are defined by using dry etching as illustrated in Fig. 1 (c). The deposited SiNx film buries the sloped sidewall of the recessed area. This groove surrounded by the SiN_x spacer defines the place of gate electrode. Gate oxide film is grown after cleaning on the open area and CVD poly-Si film is deposited and planarized by CMP, as shown in Fig.1 (d), to define the gate electrode within the groove. SiN_x is removed as illustrated in Fig. 1 (e). As shown in Fig.1 (f), the device fabrication is completed using a conventional fabrication sequence including salicided source/drain and gate electrode.

3. Results and Discussion

Devices were fabricated using a baseline 0.25μm photolithography on SOI wafers with 100nm buried oxide thickness. Fig.2 shows a X-SEM view of the fabricated MOSFET. The MOSFET's dimensions were; 25nm as recessed channel thickness, 50nm as source/drain thickness, 2nm as gate oxide, 0.15μm as bottom gate length and 0.20μm as top gate length. By using this process, 0.25μm gate length was shrunk to 0.15μm. As shown in Fig.2, the polysilicon gate was self-aligned-formed on the recessed channel.

Fig.3 (a) and (b) shows V_g-I_d and V_d-I_d characteristics, respectively, of nMOSFET with L/W=1.0/10μm (designed), or 0.9/10μm (actual). The sub-threshold slope was 63mV/dec. V_{th} was around –0.18V. As shown in Fig.3 (b), I_{dsat} was 219μA/μm at V_d=V_g=1.0V. Fig.4 shows V_d-I_d characteristics of nMOSFET with L/W=0.25/10μm (designed), or 0.15/10μm (actual). I_{dsat} was 674μA/μm at V_d=V_g=1.0V. Close to ideal sub-threshold slope and kink-free characteristics in Figs.3 and 4 confirm fully depleted operation of the proposed devices.

The sheet resistance of the source and drain with 35nm-thick-$TiSi_2$ was 6.2ohm/sq. This value is reasonable for 0.1μm SOI MOSFET. As 35nm-thick-$TiSi_2$ needs about 35nm-thick sacrificial Si, it is impossible to get this resistance for 25nm-thick-source/drain.

4. Conclusions

We successfully fabricated the SOI MOSFET with self-aligned gate on recessed channel region. This process was carried out by using conventional CMOS bulk process and without the influence of thermal budget or facet like SEG process. This structure and process enables to reduce the parasitic resistance of source/drain and to scale down the channel thickness and the gate length of sub-0.1μm CMOS transistors.

References

[1] The International Technology Roadmap for Semiconductor (2001)

[2] Jong-Ho Lee, et al., *Proc. 1996 IEEE International SOI Conference, Oct. 1996* (1996) p. 122.-

[3] M. Chan, et al., IEEE Electron Device Letters, Vol. 15, No. 1, January (1994) p.22

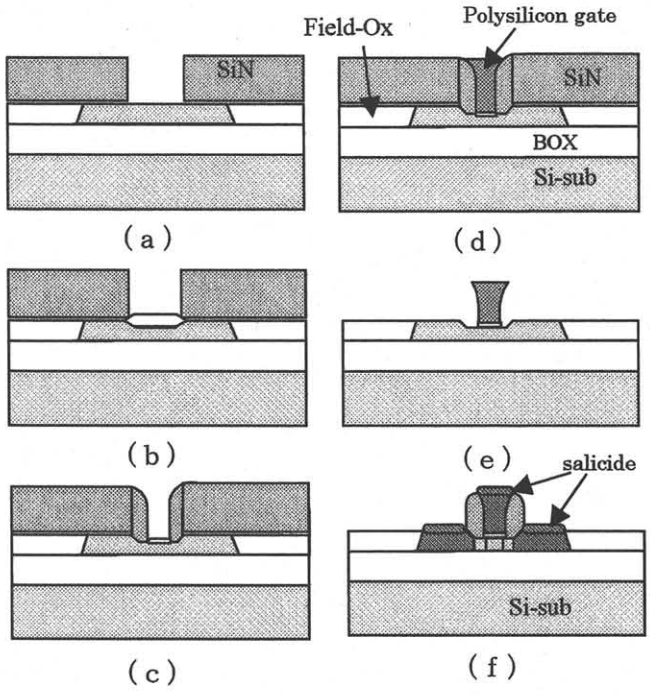

Fig.1: Illustration of process flow of FD-SOI MOSFET with self aligned gate formed on recessed channel

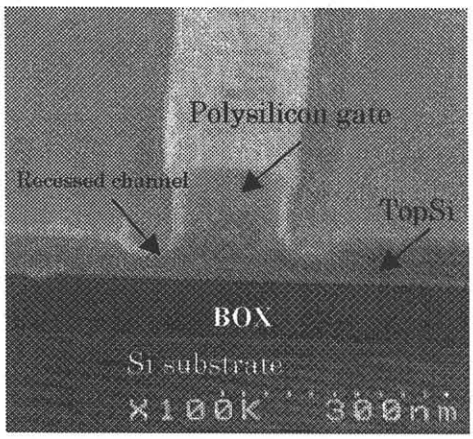

Fig.2: X-SEM image of recessed channel and self-aligned gate with over-hang shape.

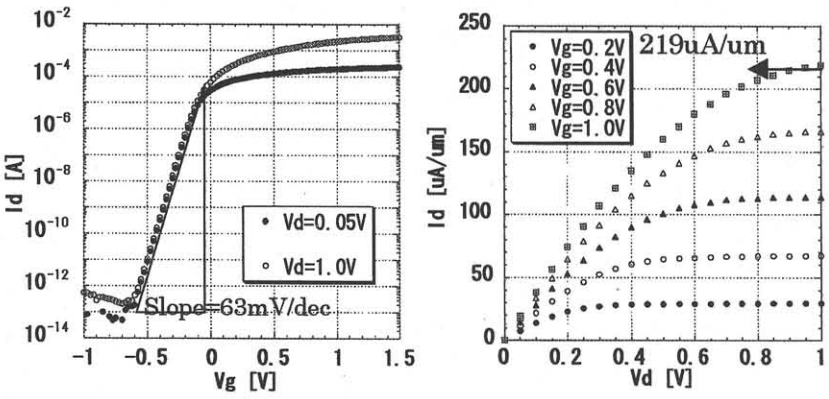

Fig.3(a), (b): V_g-I_d and V_d-I_d characteristics, respectively, of nMOSFET with L/W=1.0/10μm(designed)

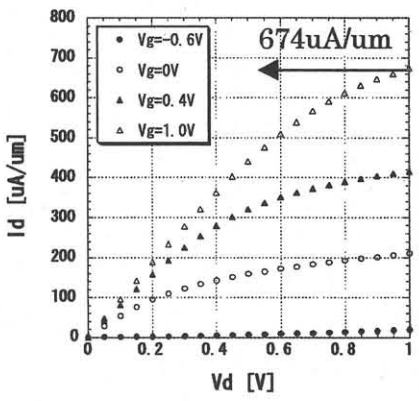

Fig.4: V_d-I_d characteristics of nMOSFET with L/W=0.25/10μm (designed), or 0.15/10μm (actual)