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Hot-Carrier-induced Degradation on 0.1μm Partially Depleted SOI CMOSFET with thin Oxide

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1. Introduction

Partially Depleted SOI MOSFET (PD-SOI) was an attractive device due to the advantages such as full dielectric isolation and reduced junction capacitance which over bulk-Si device [1-2]. As technology was scaled down to 0.1μm regime, a study of hot-carrier injection was needed to predict the long-term reliability of 0.1μm SOI devices with thin oxide (~2nm). This work investigates hot-carrier-induced degradation of 0.1μm PD-SOI device at various applied voltage as well as temperatures with respect to body-contact SOI (BC-SOI) with body contacted and floating-body SOI (FB-SOI) CMOSFETs.

2. Experiments

PD-SOI CMOSFET devices on IMplanted Oxygen (SIMOX) SOI substrates were fabricated with 190nm thick Si active layers, 150nm thick buried oxide (BOX), and 2nm nitride gate oxides using the 0.1μm process. Device HCE stressing and measurements were performed on probe stations using various drain voltages (V_D=1.2~2.4V), gate voltages (V_G=0~2.4V) and temperatures (25 ~ 125°C) with 100min stress time

3. Results

Figure 1 shows the I_D-V_D characteristic of 0.1μm FB-SOI and BC-SOI nMOSFETs, which was stressed under constant drain and gate voltages (V_D=V_G=2.4V). The FBE happen on FB-SOI (Fig. 1b) and can be suppressed by body contact using T-gate structure [3] on BC-SOI (Fig. 1a). It is apparently that I_{Dsat} degradation of BC-SOI was larger than that of FB-SOI. The subthreshold swing of 0.1μm BC-SOI (Fig. 2a) and 0.1μm FB-SOI (Fig. 2b) was degraded after stressing and become more serious as gate stress increases. It indicates interface trap creation causes subthreshold slope degradation, resulting in a threshold voltage change. Figure 3 shows the time dependent degradation on I_{Dsat} for both SOI nMOSFETs. For 0.1μm BC-SOI nMOSFET with thin oxide (~2nm), channel holes are created at larger V_G due to valence-band electron tunneling [4], accelerating interface trap generation rate. Therefore, larger I_{Dsat} degradation of BC-SOI at first is happen on maximum I_{sub} at V_G=V_D/2 due to impact ionization, then higher valence-band electron tunneling occurred apparently on V_G=V_D enhances interface state generation rate to result the maximum I_{Dsat} degradation (Fig. 3a). For 0.1μm FB-SOI with FBE, larger I_{Dsat} degradation is happened on (V_G~V_T) due to the parasitic bipolar effect (PBT), as shown in Fig. 3b. As the PBT action is activated, hot holes are generated by impact ionization, resulting in the interface defects generation. Thus, initial hot-carrier-induced I_{Dsat} degradation in FB-SOI nMOSFET is enhanced by PBT when V_G~V_T. Then valence-band electron tunneling occurs at V_G=V_D, resulting in maximum I_{Dsat} degradation.

As ambient temperature was increased, I_{Dsat} degradation was suppressed (especially at V_G=V_D/2) due to the occurrence of phonon scattering, reducing channel electron mobility and impact ionization rates. Thus for BC-SOI nMOSFETs at high temperature, maximum I_{Dsat} degradation always occurred when V_G=V_D (Fig. 4a), because of many electron-hole generation enhances electron tunneling at higher V_G, cause lots of interface states leading to maximum I_{Dsat} degradation. In 0.1μm FB-SOI nMOSFETs at room temperature, electron and hole injection occurred at V_G~V_T because of PBT. But the FBE was less severe at high temperature due to self-heating effect, which produces an increase number of phonons available to assist a scattering, shortening the mean-free-path of the channel carriers. Thus, maximum I_{Dsat} degradation was happened on V_G=V_D stressing (Fig. 4b). In this work, the hot-carrier-induced I_{Dsat} degradation at V_G=V_D in FB-SOI devices was inversely temperature-dependent compared to BC-SOI devices. After V_G=V_D stressing at room temperature, BC-SOI nMOSFETs shows reduced subthreshold behavior and larger gate-induced drain leakage (GIDL) measured at V_G= -0.6V (Fig. 5a). GIDL is a direct result of the generation of interface states [5]; thus, maximum I_{Dsat} degradation occurred upon the maximum increase in interface state. As ambient temperature was increased, device subthreshold slopes deteriorated and GIDL increased due to electron-hole generation. Thus, the I_{Dsat} was degraded serious after hot carrier stressing at V_G=V_D. For FB-SOI nMOSFETs after V_G=V_D stressing at room temperature, device subthreshold slope was deteriorated and substrate-to-drain potentials were also reduced due to FBE; thus, GIDL decreased as gate stress increased, (Fig. 5b). But increasing temperature suppresses FBE, the I_{Dsat} degradation of stressed FB-SOI nMOSFETs at high temperature exhibiting worse subthreshold characteristics and larger GIDLs. It is believed that more interface states occurred at at V_G=V_D due to electron-hole generation, resulting in maximum I_{Dsat} degradation.

For 0.1μm FB-SOI pMOSFET, FBE is insignificant because of the less impact ionization with lower channel hole mobility. Thus, there is no obvious difference of hot-carrier-induced I_{Dsat} degradation between BC-SOI (Fig. 6a) and FB-SOI (Fig. 6b). Experimental results show that there is no apparent subthreshold swing degradation happened on both 0.1μm SOI devices (Fig. 7). The time dependent degradation in I_{Dsat} for 0.1μm SOI pMOSFETs was investigated. The worst stress condition on 0.1μm BC-SOI pMOSFET was occurred on V_G=V_D (Fig. 8a), which due to higher valence-band hole tunneling occurred apparently on thin oxide pMOSFET enhances interface generation rate to result the maximum I_{Dsat} degradation. Without obvious FBE, the maximum hot-carrier-induced I_{Dsat} degradation of 0.1μm FB-SOI pMOSFET was also occurred on V_G=V_D (Fig. 8b). As ambient temperature was elevated, I_{Dsat} degradation was increased due to the occurrence of electron-hole generation, enhancing valence-band electron tunneling resulting in interface states occurred especially at V_G=V_D. Thus maximum I_{Dsat} degradation at high temperature always occurred when V_G=V_D for both SOI pMOSFETs (Fig. 9a, 9b). The temperature dependence of hot-carrier–induced degradation on FB-SOI pMOSFET was same as that on BC-SOI pMOSFET. For pMOSFETs after V_G=V_D stressing at room temperature, there is no apparent degradation on device subthreshold slope. But increasing temperature, device subthreshold characteristic was deteriorated (Fig. 10a, 10b). It is believed that more interface states occurred at high temperature because of higher valence-band hole tunneling, resulting in maximum I_{Dsat} degradation.

4. Summary

For BC-SOI nMOSFET, higher valence-band electron tunneling leading to maximum hot-carrier-induced I_{Dsat} degradation on V_G=V_D. But for FB-SOI nMOSFET, initial I_{Dsat} degradation is enhanced by PBT when V_G~V_T. Then maximum I_{Dsat} degradation occurs at V_G=V_D due to electron tunneling. FB-SOI devices were inversely temperature-dependent compared to BC-SOI devices. For pMOSFET, the impact ionization was not obvious due to lower channel hole mobility; thus, the maximum I_{Dsat} degradation was occurred on V_G=V_D for both SOI pMOSFET.

Acknowledgement

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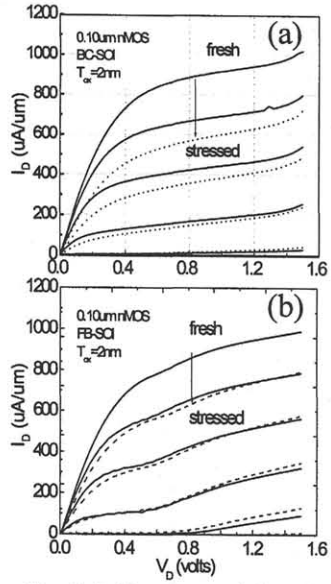

Fig. 1. I_D-V_D characteristics of 0.1μm (a) BC-SOI and (b) FB-SOI nMOSFETs before and after stressing.

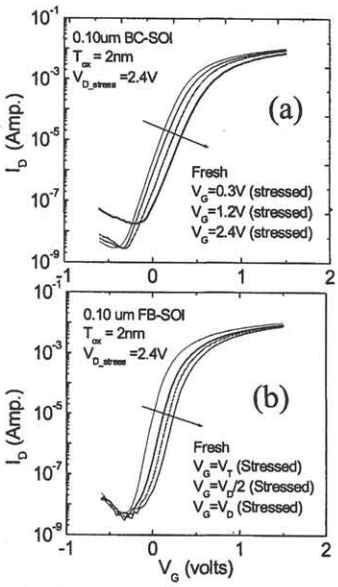

Fig. 2. I_D-V_G characteristics of 0.1μm (a) BC-SOI and (b) FB-SOI nMOSFETs before and after stressing.

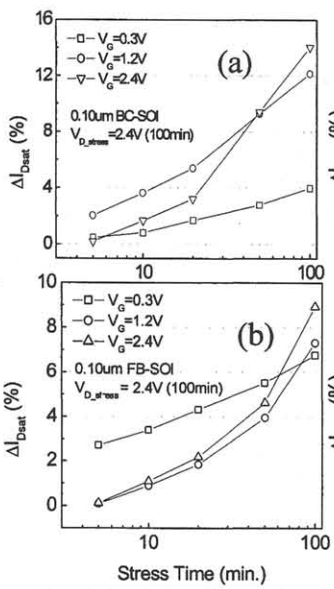

Fig. 3. I_{Dsat} degradation vs. stress time with the different stress V_G on 0.1μm (a) BC-SOI and (b) FB-SOI nMOSFETs.

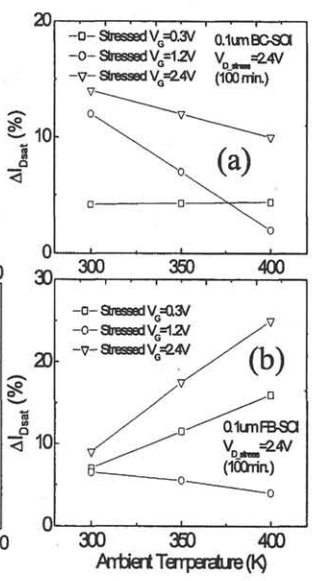

Fig. 4. I_{Dsat} degradation as a function of ambient temperature in 0.1μm (a) BC-SOI and (b) FB-SOI nMOSFETs.

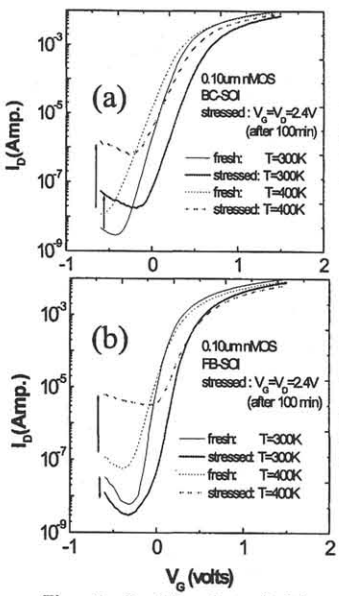

Fig. 5. I_D -V_G plot of 0.1μm (a)BC-SOI and (b)FB-SOI nMOSFETs before and after stressing at different Temperature.

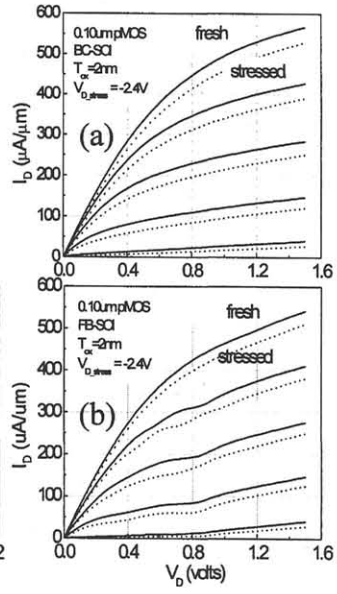

Fig. 6. I_D-V_D characteristics of 0.1μm (a) BC-SOI and (b) FB-SOI pMOSFETs before and after stressing.

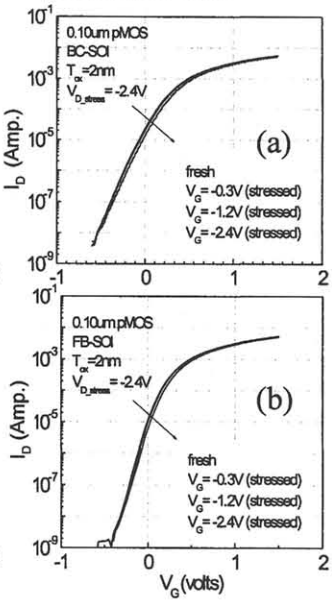

Fig. 7. I_D-V_G characteristics of 0.1μm (a) BC-SOI and (b) FB-SOI pMOSFETs before and after stressing.

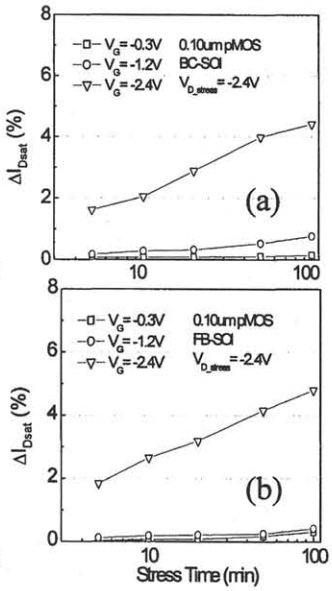

Fig. 8. I_{Dsat} degradation vs. stress time with the different stress V_G on 0.1μm (a) BC-SOI and (b) FB-SOI pMOSFETs.

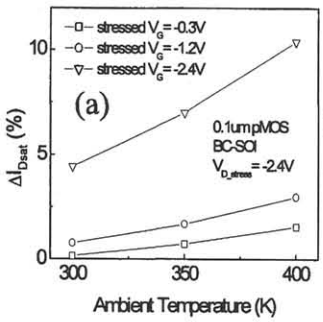

Fig. 9. I_{Dsat} degradation as a function of ambient temperature in 0.1μm (a) BC-SOI and (b) FB-SOI pMOSFETs.

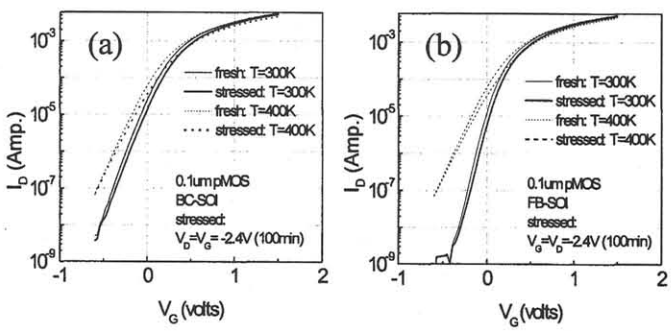

Fig. 10. I_D -V_G plot of 0.1μm (a) BC-SOI and (b) FB-SOI pMOSFETs before and after hot-carrier stress at different ambient temperatures.