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Grain-Boundary Related Hot Carrier Degradation Mechanism
in Low-Temperature Poly-Si Thin-Film-Transistors

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1. Introduction

For realization of "system-on-panel" which is one of the next-generation systems in the great expectation, the role of low-temperature (LT) poly-Si thin-film-transistors (TFTs) is important, since high-speed circuits such as processors, memories, drivers, and so on need to be integrated with a pixel array on the same glass or plastic substrate. To achieve this, further advances of performance and reliability of LT poly-Si TFTs are strongly required.

With recent remarkable progress of device fabrication processes, LT poly-Si TFTs with a high performance have been successfully obtained on glass or plastic substrates [1-3]. However, although hot carrier reliability in LT poly-Si TFTs is one of concerned subjects, its degradation mechanism has not been well-understood.

In this paper, grain-boundary related hot carrier degradation mechanism is proposed, based on detail analyses of device characteristics before and after hot carrier stress.

2. Experimental

LT-poly-Si TFTs used in this study were fabricated as follows; Buffered SiO_2 and 50 nm-thick amorphous silicon layers were deposited by plasma-enhanced chemical-vapor-deposition (PE-CVD) on a glass substrate. After dehydrogenation annealing, XeCl-Excimer-Laser-Crystallization (ELC) was performed by the overlapping scan mode. A 120 nm-thick gate oxide was deposited by PE-CVD. Al was used as a gate electrode. And XeCl-excimer-laser was also used for activation process of ion-doped source/drain regions. The maximum process temperature was kept below 450°C. Poly-Si film under the gate in the channel regions remains undoped. The channel length was 7 μm and the channel width was 5 μm.

Hot carrier stress was performed at a gate voltage (V_G) of 3 V and a drain voltage (V_D) of 10 V for 20 min in the dark. The gate voltage is the condition showing the maximum body current at V_D=10 V, due to impact ionization near the drain (during the stress, the body region was electrically floating).

3. Results and discussions

Figures 1 (a) and 1 (b) show the I_D-V_G curves in normal and reverse (the source and drain interchanged) modes, respectively. The solid and dashed lines shows results before and after stress. Measurements were carried out under various values of V_D. Both figures indicate that a large amount of negative charge was generated after stress, which causes a strong degradation of drain current. From these figures, it can be seen that the I_D-V_G characteristic was recovered to the initial one with the increase in V_D in the normal mode, while no recovery can be seen in the reverse mode. This indicates that the negative charge was induced close to the drain edge after stress.

Another remarkable phenomenon can be seen at the V_G region of less than 1 V. In this region, the drain current after stress shows almost the same value as the initial one, which is different from a phenomenon caused by conventional interface traps between the gate oxide and the poly-Si body. Figure 2 shows charge-pumping (CP) characteristics before and after stress. The height of the pulse gate voltage was 4 V, and the frequency was 250 kHz in the measurements. There is no significant difference between the CP characteristics before and after stress, which means that interface traps between the gate oxide and the body little increase after stress.

To explain the drain current degradation due to hot carrier stress, a hot-carrier-induced resistance R_I is introduced near the drain as shown in Fig. 3 (a), which is connected in series with channel resistance $R_{channel}$. In the low V_G condition, the $R_{channel}$ is still high so that the R_I can be neglected, which results in good agreement of I_D-V_G characteristics before and after stress, as shown in Fig. 1. Figure 3 (b) shows R_{SD} vs. V_G curves before and after stress, where R_{SD} is a resistance between the source and drain. R_I values were calculated by subtracting R_{SD} values before stress from R_{SD} values after stress, assuming that $R_I = 0$ Ω before stress. Figure 3 (c) shows V_G and V_D dependences of R_I. V_D was changed from 0.1 V to 4.0 V in 0.3 V step. From this figure, it can be seen that R_I values are systematically decreased with the increase in V_D, which also indicates that the degraded region is close to the drain edge. Moreover, the R_I values show the exponential decay with the increase in V_G, which imply lowering of a potential barrier.

A possible model to explain these results is the generation of negative charges at grain boundaries degraded by hot-carrier-attack. The degraded region is close to the drain edge near the surface. As schematically shown in Fig. 4 (a), carriers flow deeper from the surface with the increase in V_D, resulting in the small effective R_I value. The potential barriers for carriers caused by the negative charges at grain boundaries are reduced by the increase in V_G as roughly shown in Fig. 4 (b), which also results in the decrease of R_I value

4. Summary

Unique degradation behavior in I_D-V_G characteristics was observed in LT poly-Si TFTs after hot carrier stress. It can be explained by generation of negative charges at grain boundaries close to drain edge near the surface after stress.
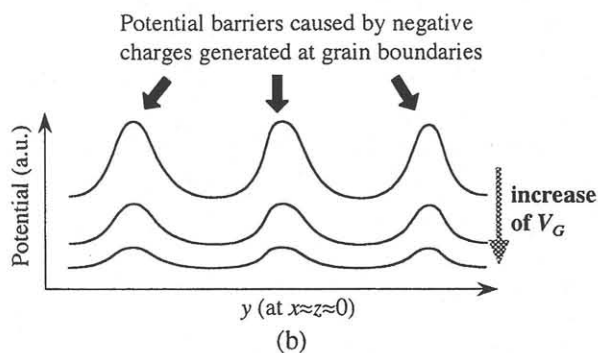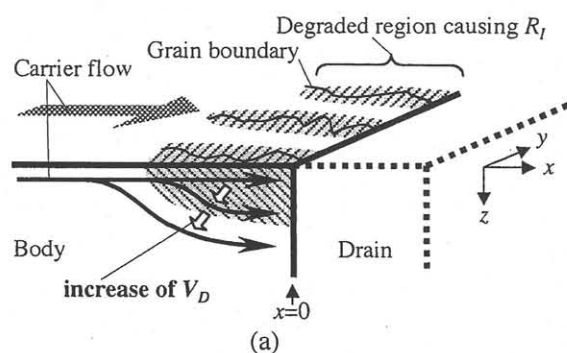
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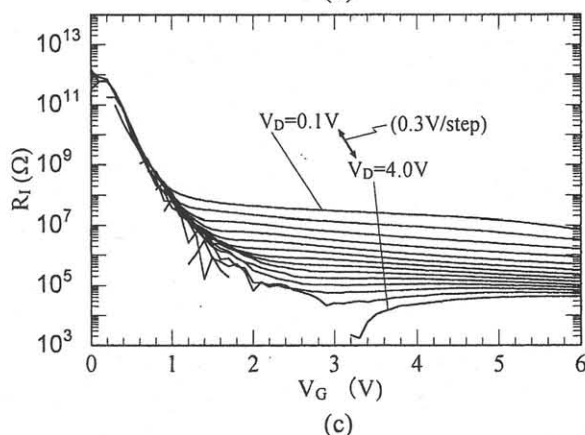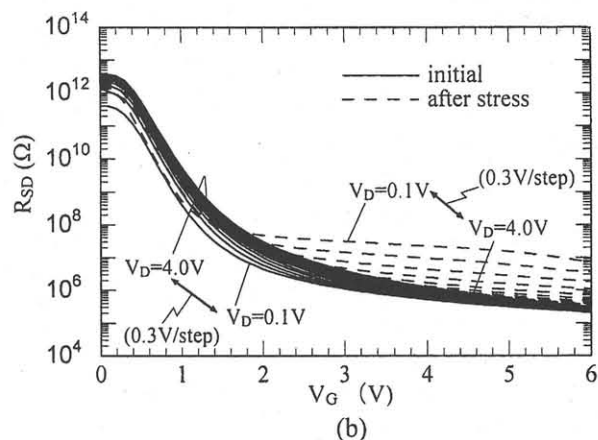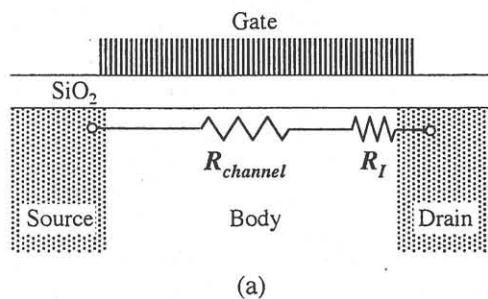[3] S. D. Theiss et al., Tec. Dig. IEDM (1998) p.257.
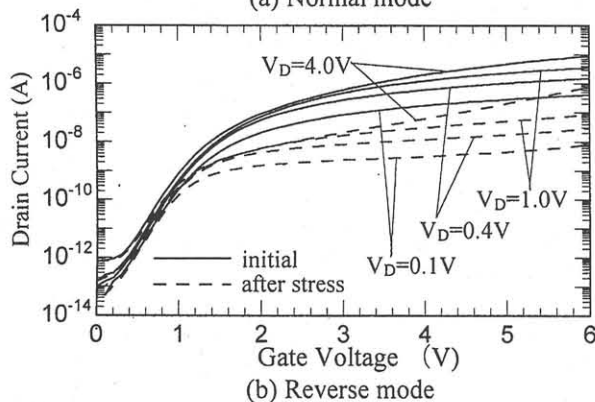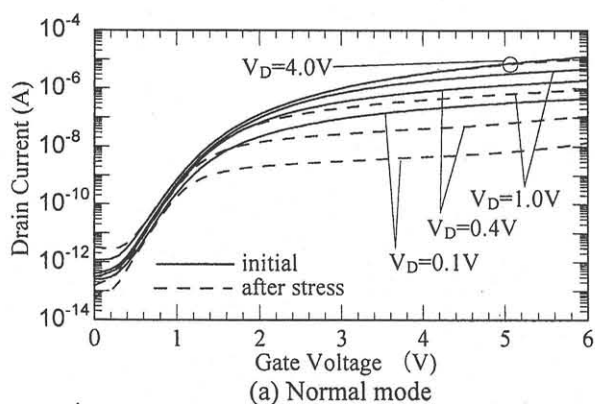
Fig. 1 I_D-V_G curves before and after stress in (a) normal mode and (b) reverse mode.
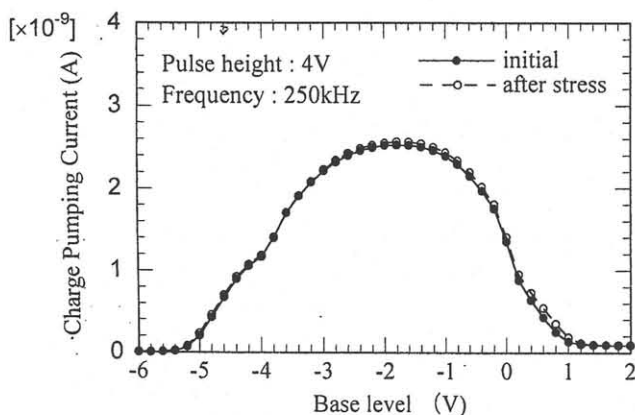
Fig. 2 Charge pumping characteristics before and after stress.

Fig. 3 (a) An illustrated resistance model of TFT after stress. (b) Source-drain resistance values R_{SD} ($=R_{channel}+R_I$) before and after stress. (c) V_G and V_D dependences of calculated hot-carrier-induced resistance values R_I.

Fig. 4 An explanation model for R_I behaviors; (a) V_D dependence and (b) V_G dependence.