Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 272-273

E-1-2

InP Double-Heterojunction Bipolar Transistors with a Carbon-Doped Graded Base

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1. Introduction

In the last several years, InP heterojunction bipolar transistor (HBT) technologies have made steady progress toward commercial application to 40-Gbit/s fiber optic communications. Today, the research concern has shifted to building over 100-Gbit/s ICs by extracting the ultimate high-speed potential of devices. Vertical epitaxial layer structures [1], deep submicrometer lateral scaling [2], dynamic operation of digital ICs [3], and other strategies are being investigated as ways to achieve this goal.

For vertical epitaxial layer structures, thinning the base and collector layers is effective in reducing the carrier transit time. It is also quite effective in increasing the current density available for device operation [1]. However, this approach adversely increases the base resistance and collector capacitance, which results in an increase in the *RC* charging time. The *RC* delay associated with the load resistance and collector capacitance can be reduced by increasing the bias current. However, the *RC* delay arising from the base resistance cannot be alleviated by increasing the current. Thus, it is still important to reduce the base resistance by optimizing the vertical-layer design (although aggressive lateral scaling is the ultimate solution to decreasing the total *RC* charging time [2]).

This paper reports compositionally graded-base structures established by using pseudomorphic $In_xGa_{1-x}As$ ($x < 0.53$). The graded-base design is useful in alleviating the tradeoff between the base resistance and current gain [4]. Additionally, a larger GaAs mole fraction enhances the *p*-type dopant incorporation into the epilayers, which is also important in achieving lower base resistance. In this work, we investigated the performance of the HBTs designed for 100-Gbit/s applications and did a HSPICE simulation to examine the propagation delay of emitter-coupled logic (ECL) gate.

2. Device Structure and Fabrication

Double-heterojunction structures were grown on 3-inch InP substrate by metalorganic vapor phase epitaxy with carbon as a *p*-type dopant. The collector is 200-nm thick and consists of step-graded InGaAs/InGaAsP layers and a thicker InP to obtain sufficiently large breakdown voltage. For the base, we prepared two types of graded structures, GB-1 and GB-2, as shown in Fig. 1. For GB-1, GaAs fraction is monotonically increased from 0.47 to 0.54 toward the emitter/base heterointerface. Its thickness is 35 nm. On the other hand, GB-2 employs a two-step grading across the 50-nm-thick layer to alleviate the lattice-mismatch strain. Here, higher built-in field is set near the heterointerface to effectively sweep the scattered electrons out to the collector. The carbon concentration is ~6×10^{19} cm^{-3} for both structures. The device layout and fabrication process are the same as reported elsewhere [1]. The emitter is 0.8-μm wide and 3-μm long. The "base-pad isolation" technique was utilized to reduce the external collector capacitance. To reverse the hydrogen passivation, 500°C annealing was carried out during the process. The base sheet resistances are 487 Ω for GB-1 and only 314 Ω for GB-2. The base contact resistances are only less than 5 Ωμm^2 for both structures.

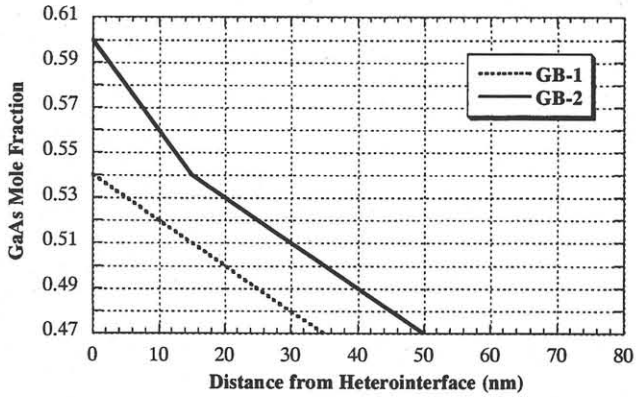

Fig. 1. GaAs fraction in the $In_xGa_{1-x}As$ base designed for this work.

3. Device Performance

Figure 2 shows the collector *I-V* characteristics of the fabricated HBTs. The collector breakdown voltage of over 5 V is obtained even with the 200-nm collector. Simultaneously, high current injection of over 3 mA/μm^2 is achieved without any current blocking effect. These results reflect the proper arrangement of the conduction-band potential profile in the step-graded collector.

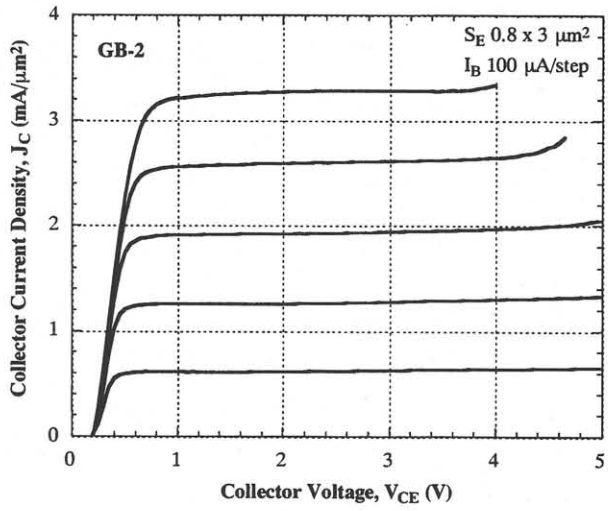

Fig. 2. Typical collector *I-V* characteristics for the GB-2 structure.

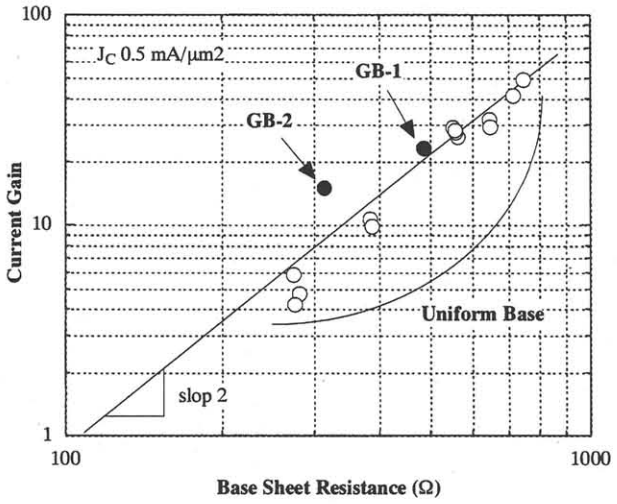

Fig. 3. Current gain versus base sheet resistance. The current gains for uniform-base structures are also shown for comparison.

Figure 3 plots current gain against base sheet resistance. The current gains for uniform-base HBTs are also shown for comparison. As seen from the figure, GB-1 exhibits almost the same current gain (~23) as the uniform-base structures. This means that the graded-base design is not useful in upgrading the transport properties for a thin base (< 30 nm). In contrast, GB-2 shows more than 60% increase in current gain (~15) compared with its uniform-base counterparts. It is thus concluded that the graded-base design is particularly suited to moderate layer thickness (~50 nm) and is therefore useful in minimizing the base sheet resistance.

The f_t and f_{max} were determined from h_{21} and unilateral gains, respectively. The results are shown in Fig. 4. GB-2 exhibits peak f_t of 224 GHz and peak f_{max} of 317 GHz at J_C of 2.5 mA/μm^2, while GB-1 offers f_t of 259 GHz and f_{max} of 288 GHz. Apparently, the high f_{max} value for GB-2 originates from the low base sheet resistance achieved by the high base doping and moderate base thickness. Figure 4 also shows the dependence of f_t and f_{max} on collector bias voltage at J_C of 2 mA/μm^2. Good turn-on behavior against the bias voltage is confirmed. The f_{max} of over 250 GHz is obtained even at V_{CE} of only 1 V (V_{CB} ~ 0 V).

We extracted transistor parameters using measured *s*-parameters and the device geometry. For GB-2, the extracted transit time is 0.40 ps, base resistance 25 Ω, and total collector capacitance 7.9 fF. The ratio of the external to internal collector capacitances is around 1 in the active bias region. The average electron velocity in the base and collector is 3.7 x 10^7 cm/s, and the transit time constitutes 60% of the total delay time. Based on the extracted transistor parameters, we also conducted HSPICE simulation on ECL ring oscillators to estimate the gate propagation delay t_{pd}. The result shows t_{pd} of 2.5 ps when the logic swing of 0.3 V and the transistor bias current of 6 mA (2.5 mA/μm^2) is assumed. This value is small enough to project the possibility of 100-Gbit/s ICs.

4. Conclusion

In summary, we have investigated the performance of InP HBTs featuring an $In_xGa_{1-x}As$ graded base. The HBTs with a 50-nm-thick base exhibit more than a 60% increase in current gain compared with the uniform-base structures. They also exhibit f_t of

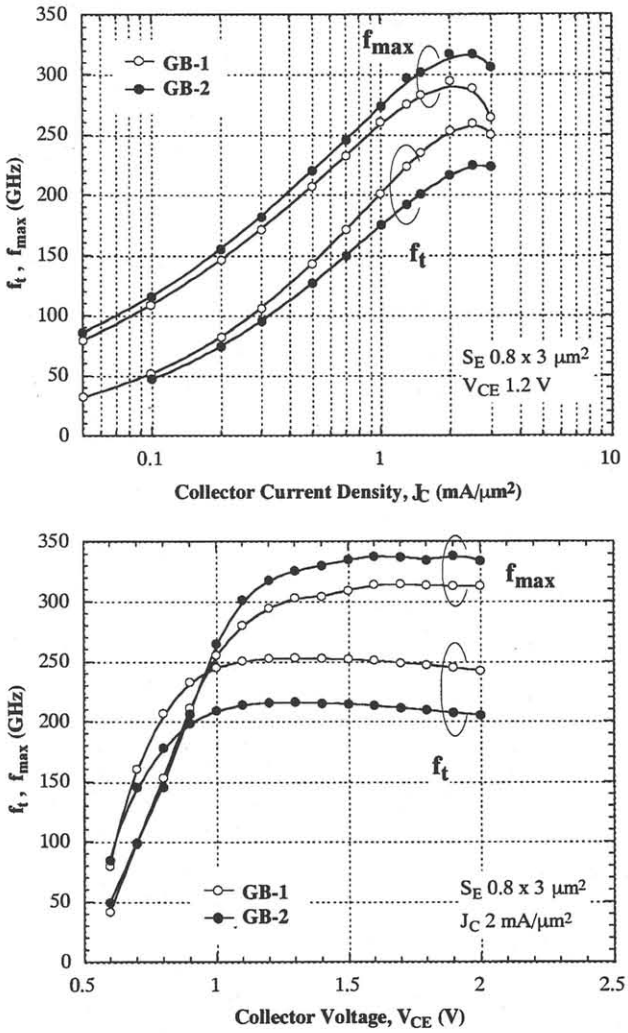

Fig. 4. Typical collector bias dependences of f_t and f_{max}.

over 200 GHz and f_{max} of over 300 GHz simultaneously at V_{CE} of 1.2 V and J_C of 2 mA/μm^2. The HSPICE simulation predicts ECL-gate delay of 2.5 ps for 0.3-V logic swing.

Acknowledgments

We thank T. Enoki, K. Ishii, and H. Nosaka for their advice. Special thanks are due to H. Niiyama and M. Fujisaki for their assistance.

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