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GaAs on Si Technology and Its Application to Power Amplifiers

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1. Introduction

Compound semiconductors are one of the key materials, which have enabled the communications revolution of today, and components manufactured from compound semiconductors are to be found at the heart of most high technology systems, including optical fiber communication systems, wireless communication and mobile phone systems, satellite communications and power supplies, data storage systems (CD, CD-ROM and DVD), barcode scanners, outdoor displays, traffic signals and many new developments in the medical and automotive industries.

Many of these uses are large volume consumer applications which are very sensitive to the manufacturing cost. As the GaAs device volumes have risen, the manufacturing processes have become more efficient so that the cost of the materials represents a significant portion of the device manufacturing cost. For example, the implementation of large volume epitaxial tools have allowed the cost of epitaxy to be reduced so that the substrate cost represents over 50% of the price of the epitaxial wafer.

IQE working in cooperation with Motorola's Physical Science Research Labs have developed a technique that allows III-V epitaxial layers to be grown on top of Si substrates which results in a significant reduction to the cost of an epitaxial wafer. Although many research groups have reported on efforts making GaAs on Si devices, we believe this technology is unique as it allows good performance while still maintaining the cost advantage inherent of the use of the Si substrate.

2. Results

This approach is unique in the fact it uses a thin layer of single crystal $SrTiO_3$ (STO) between the Si substrate and GaAs epilayers. The lattice constant of the STO is approximately halfway between that of Si and GaAs allowing step grading between the two dissimilar materials.

The epitaxial growth is conducted via molecular beam epitaxy (MBE). The Si substrates are placed within the vacuum chamber where the native oxide is desorbed. Single crystal STO is then epitaxially grown on the Si substrate. During the initial growth of the STO, oxygen diffuses to the interface forming an amorphous SiO2 layer between the Si substrate and STO. This amorphous region allows the STO to quickly relax to its normal lattice constant that is about 2% mismatched to GaAs. The GaAs device structure is then grown on top of the relaxed STO. A TEM cross-section is shown in Figure 1 below.

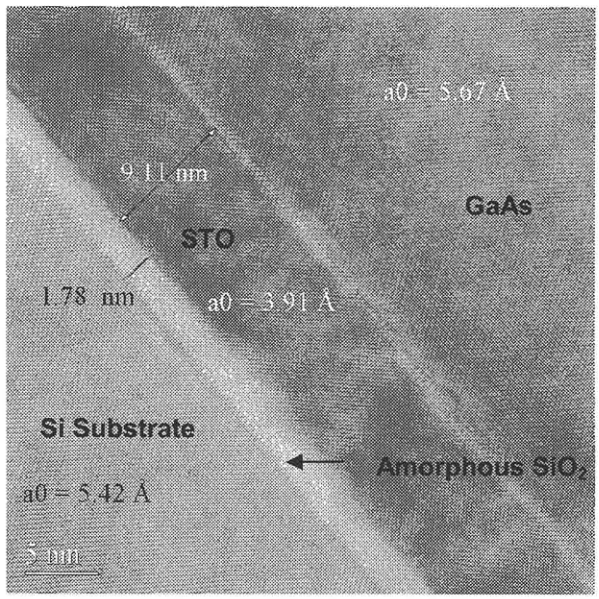

Figure 1 TEM Cross-Section

Initially 0.7um. GaAs MESFET devices were manufactured using both the GaAs/STO/Si technology as well as a GaAs control. The saturation current at 0.5V forward gate bias is 367 ma/mm and 385 ma/mm for the GaAs/STO/Si and GaAs control respectively. The maximum transconductance is 223 ms/mm and 240 ms/mm for the GaAs/STO/Si and GaAs control respectively.

Power PHEMT structures using double planar doping were also fabricated using the same 0.7 um

recessed gate process. The saturation current at 2V drain source bias is 899 ma/mm and 930 ma/mm for the GaAs/STO/Si and GaAs control respectively. The maximum transconductance is 537 ms/mm and 535 ms/mm for the GaAs/STO/Si and GaAs control respectively. The room temperature mobility was within 91% of the control while the saturated electron velocity was within 84% of the control. AFM images indicated the RMS value of the surface roughness to be less than 10 Á for the GaAs/STO/Si wafers.

The MESFET wafers have been fabricated using a 3mm gate width device design. The small signal performance from sample devices is shown in Figure 2.

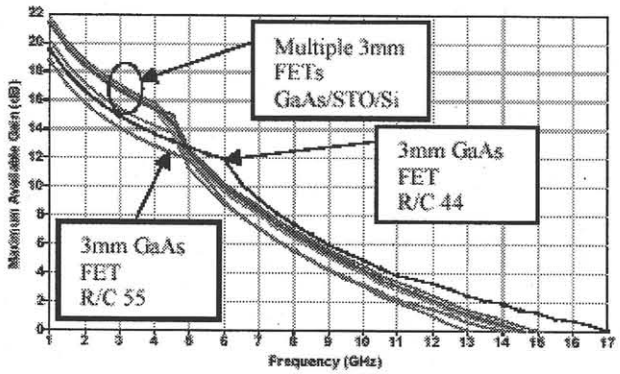

Figure 2 Maximum Available Gain vs Frequency

The MESFET devices have been tested and used in functioning mobile phone handsets. The corresponding power characteristics are shown below in Figure 3.

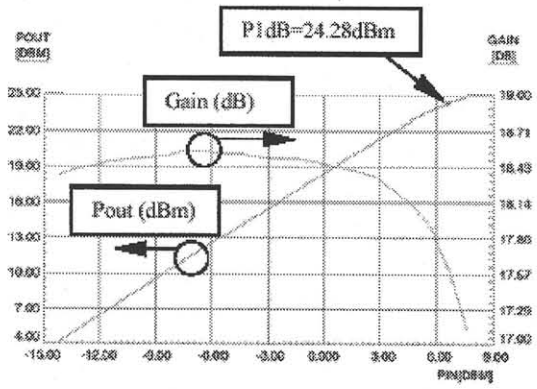

Figure 3 Gain and Pout vs Pin for 3mm MESFET device

3. Conclusion

A novel approach to growing GaAs on Si has been demonstrated using an intermediate oxide layer. The resulting device performance is comparable to what one might obtain using a standard GaAs substrate. For cost sensitive applications, the use of a Si substrate will result in a significant cost savings. Furthermore, the same basic principle can be applied to other material systems where the potential cost savings may be much greater. Also new applications involving the integration of III-V devices with more mature Si circuitry may now be contemplated.