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Drain-current collapse in AlGaN/GaN HEMTs on sapphire and semi-insulating SiC substrates

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1. Introduction

Nitride-based field effect transistors are of great interest due to their capability of operating at high power, high temperature and high frequency. An important problem facing nitride-based high power microwave electronics is the presence of drain-current collapse while applying high drain voltage. Current collapse is a trap-related phenomenon that has been observed to produce a significant reduction in the drain-current of nitride-based devices [1-5]. However, Daumiller etal [6] and Simin etal [7] reported that piezo-related charge states and the source and drain resistances of the AlGaN/GaN HEMTs are responsible for the current collapse, respectively. Many authors have studied the drain-current collapse using high drain voltage dc characteristics [1,3,4] and also pulsed dc characteristics [2,5-7]. Recently, Kikkawa etal [8] showed the drain-current collapse using small frequency super-imposed dc characteristics. No comparative studies have been performed between the HEMTs on sapphire and SiC using small frequency (120 Hz) superimposed dc measurements. In this study, we report the current collapse of AlGaN/GaN HEMTs on sapphire and semi-insulating (SI) SiC substrates using ac characteristics with different drain sweep-voltages.

2. Device Fabrication

The device structures were grown by atmospheric pressure metal-organic chemical vapor deposition (MOCVD) on (0001)-oriented SI-4H-SiC and sapphire substrates. The HEMT structure consist of a thin AlN (for SiC substrate) [9-11] or GaN (sapphire substrate) [10-12] nucleation layer, followed by a 3 um insulating GaN, 7 nm undoped-$Al_{0.26}Ga_{0.74}N$, 15 nm n-$Al_{0.26}Ga_{0.74}N$ ($4x10^{18}$ cm^{-3}) and 3 nm undoped- $Al_{0.26}Ga_{0.74}N$. Before the mesa isolation with reactive ion etching (RIE), silicon dioxide was evaporated using electron beam evaporation system on HEMT structure, which was used as a mask. The ohmic contact was performed by the deposition of Ti/Al/Ti/Au (25/100/45/55 nm), which was subsequently alloyed at 760 °C for 1 min in N_2 atmosphere. Gate metal was performed by the deposition of Pd/Ti/Au (40/40/80 nm) [9-11]. Before going to deposit ohmic and gate metals, samples were dipped in concentrated HCl solution for 60 sec. Fig. 1 shows the schematic diagram of processed devices. The device dimensions are as follows: source-drain distance (L_{sd}) 10 μm; gate width (W_g) 200 μm; gate length (L_g) 2 μm, and source-gate distance (L_{sg}) 3.5 μm. Several devices with an identical dimension were used for this study.

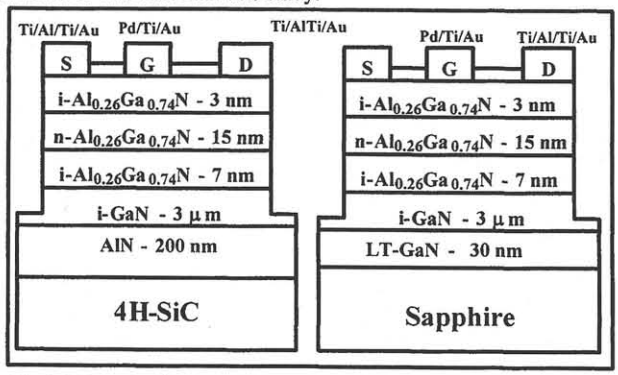

Fig.1 Schematic diagram of HEMTs on SiC and Sapphire

3. Measurements and Discussions

The dc and small frequency 120 Hz superimposed dc I_{DS}-V_{DS} characteristics (its called ac measurements) of the fabricated devices were performed using Tektronix 370A high-resolution programmable curve tracer. An ac characteristic of AlGaN/GaN HEMTs were carried out at different drain sweep-voltages (V_{DS}) of 0-4 V, 0-8 V, 0-12 V, 0-15 V and 0-20 V. Figure 2 and 3 shows the dc and ac I_{DS}-V_{DS} characteristics of AlGaN/GaN HEMTs on sapphire and SiC substrates. Though the drain-current collapse has been observed on a reproducible basis in both the HEMTs fabricated on sapphire and SiC substrates, the drain-current collapse in HEMTs on SiC is small compared with the HEMTs on sapphire substrates.

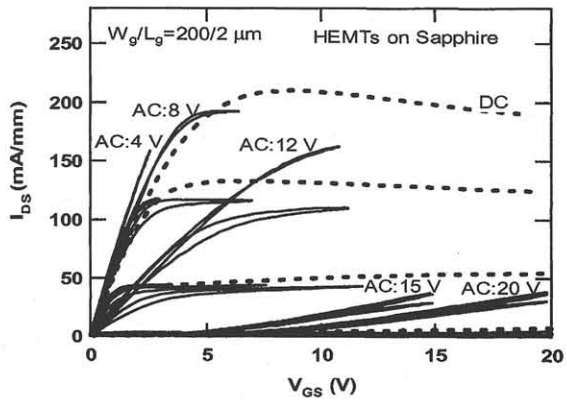

Fig.2 Measured dc and ac I_{DS}-V_{DS} characteristics (different drain sweep voltages V_{DS}= 4, 8, 12, 15 and 20 V) of AlGaN/GaN HEMTs on sapphire. Top trace was at V_{GS}=+1.5 V step voltage was -1.0 V

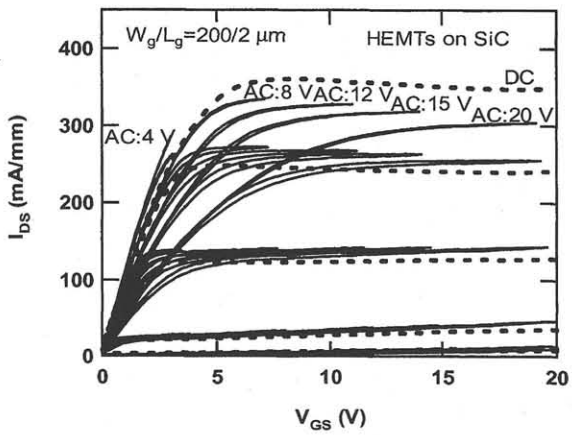

Fig.3 Measured dc and ac I_{DS}-V_{DS} characteristics (different drain sweep voltages V_{DS}= 4, 8, 12, 15 and 20 V) of AlGaN/GaN HEMTs on SI-SiC. Top trace was at V_{GS}=+1.5 V step voltage was -1.0 V

There are two ways to explain this current collapse behavior. (i) Formation of defects or the incorporation of impurities due to non-optimal growth conditions [4,5]. The current collapse occurs when a high drain-source voltage is applied to a HEMT, and hot channel carriers are injected into regions adjacent to the 2DEG channel, where they are then trapped at deep defect sites. When the high voltage is removed, the carriers remain trapped. This reduces the drain-current

and hence the output power [5]. (ii) Existence of electrical traps associated with the surface states. The current collapse was suppressed using surface-charge control process (silicon nitride passivation) [8,13]. The dc characteristics of AlGaN/GaN HEMTs on SiC [9] with a maximum saturation current about I_{DS}=850 mA/mm and the knee voltage of V_{KN}= 4.5 V at a moderate V_{DS}=30 V, would deliver an output power $P_{out} \approx 5.4$ W/mm.

In the case of RF power measurements, it is necessary to test the devices in an ac mode. Table I shows the device parameters (g_m, I_{Dmax} and V_{KN}) of HEMTs on sapphire and SiC substrates, which was obtained using dc and ac I_{DS}-V_{DS} characteristics. Small V_{KN} shift (2.31 V for drain sweep-voltage of 12 V) with small current reduction has been observed in the case of HEMTs on SiC substrate (see fig. 3). The drastic V_{KN} shift and current collapse has been observed (see fig. 2) in the case of HEMTs on sapphire substrate, which is not a desirable characteristic for high power device applications. The ac I_{DS}-V_{DS} curve of sapphire grown HEMTs shows large hysteresis width (0 to 910 mV) when compared with the HEMTs on SiC substrates (0 to 310 mV). Large value of hysteresis width is due to the presence of traps located adjacent to the channel, which raises the device capacitance.

Table I. dc- and ac-parameters of AlGaN/GaN HEMTs on sapphire and SiC substrates. Values within the brackets are measured drain-current in mA/mm at V_{KN}.

Drain sweep-voltage V_{DS}(V)	g_m (mS/mm)		I_{Dmax} (mA/mm)		V_{KN} (V) @V_{GS}=+0.5 V	
	SiC	Sapphire	SiC	Sapphire	SiC	Sapphire
4	129	63	289	159	3.06 (261)	2.86 (118)
8	133	79	334	193	4.36 (268)	3.62 (117)
12	129	66	328	163	5.26 (262)	8.0 (107)
15	123	26	319	38	6.04 (252)	-
20	116	25	304	38	9.76 (247)	-
DC	130	90	361	211	4.00 (246)	5.08 (132)

No current collapse has been observed in the HEMTs on SiC substrates except at positive gate voltages. The sapphire substrate grown HEMTs started degrading from the drain sweep-voltage of 12 V. At the sweep-voltages of 15 and 20 V, the devices were severely affected by drain-current collapse (see figure 1).

The current collapse behavior of SiC grown HEMTs are due to the existence of traps associated with the surface states [2,8,12]. But

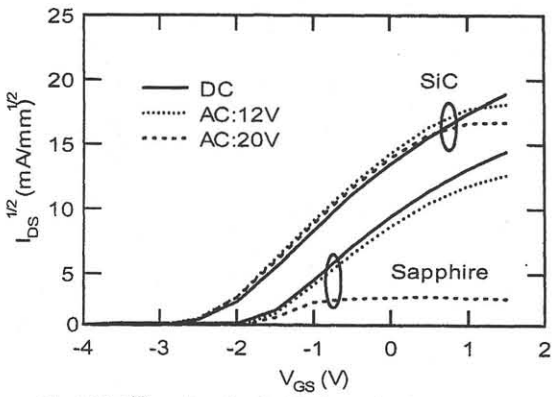

Fig.4 $(I_{DS})^{1/2}$ vs. V_{GS} plot for V_{th} determination

the drain-current collapse in sapphire grown HEMTs are due to the material defects (traps) [1,3,6] and also the surface-charge related traps. The combination of material defects (traps) and surface-charge associated traps are responsible for the severe degradation of HEMTs on sapphire substrates. It is possible to determine the location of these electrical traps by comparing the evolution of the threshold voltage for the dc and the ac characteristics. Figure 4 shows $I_{DS}^{1/2}$ vs. V_{GS} plot to determine the threshold voltage shift. No considerable threshold voltage shift was observed in the HEMTs on SiC substrates. However, threshold voltage shift was observed in the HEMTs on sapphire substrates. This argument supports the existence of material defect or traps in sapphire-based AlGaN/GaN HEMTs [2].

The extrinsic transconductance (g_m) of both the substrate grown devices decreases with the increase of drain sweep-voltages (see Table I). The increase ratio of respective parameter is small for HEMTs on SiC substrate when compared with the HEMTs on sapphire substrates. From this, it is clear that the HEMTs on SiC substrates show better ac and dc characteristics when compared with the HEMTs on sapphire substrates.

4. Conclusion

Small frequency (120 Hz) super-imposed dc I_{DS}-V_{DS} characteristics were performed on sapphire and SI-SiC grown AlGaN/GaN HEMTs. The drain-current collapse was observed on both the substrate grown HEMTs while increasing the drain sweep-voltages. The percentage of current collapse in SiC grown HEMTs was negligibly small compared with the HEMTs on sapphire substrates. Due to the drain-current collapse, decrease of g_m with the increase of drain sweep-voltage has been observed. Low drain-current collapses in AlGaN/GaN HEMTs on semi-insulating SiC substrate is due to the existence of electrical traps associated with the surface states. Due to the existence of electrical traps associated with the surface states and material defects, sapphire-based HEMTs were severely affected by drain-current collapse.

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