

E-3-1 (Invited)

SiGe BiCMOS Technology for Communication Systems

Marco Racanelli and Paul Kempf

Jazz Semiconductor
 4321 Jamboree Rd, Newport Beach, CA 92660
 Email: marco.racanelli@jazzsemi.com

1. Introduction

Several SiGe BiCMOS technology nodes exist today at commercial foundries addressing the varied needs of the communications industry. These technologies range in complexity and performance from 0.5 μm to 0.18 μm geometry and from 40 to 200 GHz Ft. As an example, Figure 1 shows technology nodes available at Jazz Semiconductor mapped across major communication end markets.

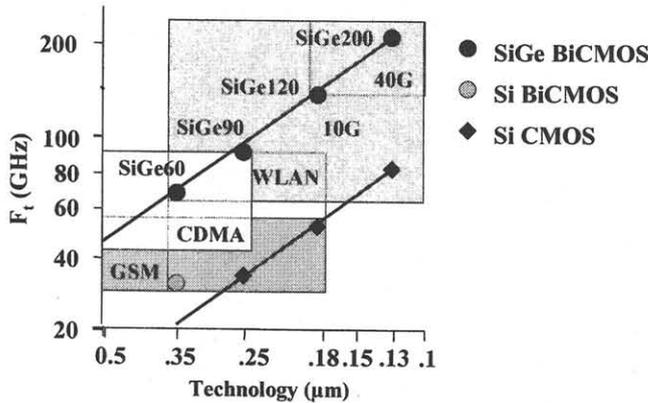


Figure 1. SiGe60, SiGe90, SiGe120 and SiGe200 represent foundry SiGe BiCMOS technology nodes. These are mapped above across major communication end markets.

In this paper, we will describe in detail a state of the art 0.18 μm , production SiGe BiCMOS process (SiGe120) and discuss tradeoffs in performance, cost, and features made in the creation of SiGe90 and SiGe200 to address different segments of the communications market as depicted in Figure 1. Together, these foundry SiGe technologies provide the means for realizing many of the transceivers of today's communication systems.

2. SiGe120

SiGe120 is a 0.18 μm , 150 GHz, SiGe BiCMOS technology targeting 10Gb and 40Gb products. Table 1 depicts specifications for the major features of SiGe120.

The process flow begins with the formation of the buried layer by a high dose implant and growth of an epitaxial layer. This approach is chosen over use of a high-energy implant to minimize collector resistance and maintain

high Ft at the low Vce typically employed in high-speed networking applications.

A deep trench is also used to reduce collector-substrate capacitance important in reducing switching delay of high-speed dividers and senders. An oxide filled shallow trench is created and dual gate oxides are formed in support of both 1.8V and 3.3V MOS transistors.

After gate formation, the bipolar is integrated by first depositing a SiGe layer using a single wafer RT-CVD reactor. A sacrificial emitter is patterned and spacers are formed to self-align the extrinsic base implant [1]. The sacrificial emitter is removed and an in-situ doped emitter is deposited such that the dimension of the sacrificial emitter exactly defines the final emitter dimension. Use of a sacrificial emitter leads to the direct patterning of the emitter dimension and thus results in a device that can be scaled more controllably than one employing techniques that rely on inside spacers. This technique also results in a self-aligned emitter-base without requiring the use of selective epitaxy. A collector implant is used to differentiate the Ft and BVceo of the three NPN transistors shown in Table 1.

Next, the CMOS devices are completed with formation of spacers, source and drain implants, and Co silicide. The back-end includes six layers of metal, a 1 fF/ μm^2 MIM capacitor, a 25 ohm/sq metal resistor and two layers of thick Al for improved inductor and interconnect performance. Figure 2 shows a SEM of a final 6 layer metal stack and some of the integrated components.

Table 1: SiGe120 Features

NPN	Beta	HS	STD	HV	
		110	110	110	
	Ft (GHz)	150	75	35	
	Fmax (GHz)	170	130	60	
	BVceo (V)	2.2	3.8	6	
		1.8 V NFET	1.8 V PFET	3.3 V NFET	3.3 V PFET
CMOS	Vt (V)	0.52	-0.44	0.62	-0.76
	Leff (mm)	0.16	0.14	0.3	0.27
	Idsat (mA/mm)	600	255	600	245
Resistors	Rs (ohm/sq)	Poly	Metal		
		245	25		
Capacitor	C (fF/mm2)	MIM			
		1			
Varactor	C (fF/mm2)	P+/N/Psub			
		2			
		dC/dV (%/V)	25		
		Q (2 GHz)	>50		

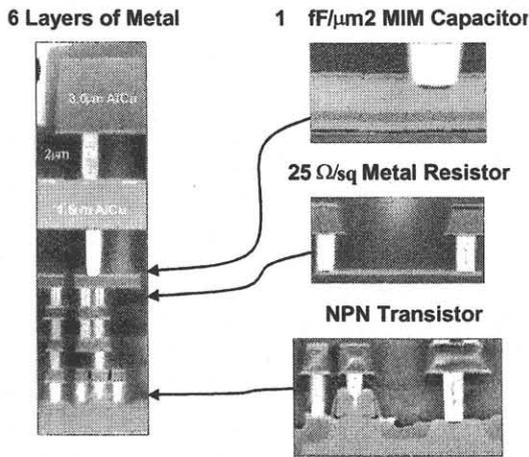


Figure 2. SEM micrograph of the SiGe120 6 metal layer stack.

3. SiGe90: Wireless SiGe BiCMOS Technology

SiGe90 eliminates features included in SiGe120 that are less relevant for wireless applications while improving some of the passive elements creating a more cost-effective wireless technology:

For handset transceivers, 1.8V CMOS is not generally required as most digital blocks are being placed on a separate base-band chip. Thus, only 3.3V FETs are included in SiGe90. Also, a transistor with 150 GHz peak Ft is not useful for 2-5 GHz applications typically operating at lower current densities and thus only the standard and high voltage transistors from Table 1 are included. Because of low parasitics, these devices still maintain a high Fmax and provide very good noise and low-current performance. Deep trench isolation is also removed as most RF blocks (outside of possibly the pre-scaler) make use of larger devices which do not benefit as much from use of deep trench and are not as sensitive to collector-substrate capacitance. The low-value, metal resistor is replaced by a high-value, poly resistor (1000 ohm/sq) and the MIM capacitor is increased to a density of 1.5 fF/μm² to reduce die cost. A 6 μm thick Al layer is also available to enable reduction of inductor size further reducing die cost.

Reference 2 details several wireless building blocks built in SiGe90. As an example, performance of a 2 GHz LNA is repeated in Table 2 below.

Table 2: Packaged, 1.96 GHz LNA measurements [2]

Ic	2.75	mA
IIP3	12.6	dB
Gain	16.2	dB
NF	0.99	dB
S11	-10	dB
S22	-19	dB

4. SiGe200: Next Generation Wire-Line Technology

To better address the needs of emerging 40Gb applications, higher Ft and Fmax are needed. Reference 1 describes how a combination of lower emitter resistance, together with a more aggressive vertical profile was used to eventually improve Ft to 200 GHz without change in device architecture thus re-using much of the mature process flow already in production with SiGe120.

Fmax is improved primarily through device scaling which reduces base resistance and collector capacitance. Figure 3 shows the result where both Ft and Fmax of >200 GHz are demonstrated.

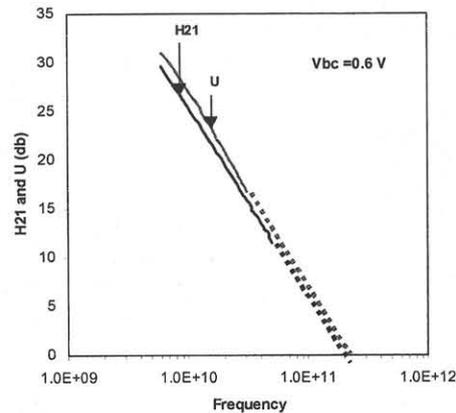


Figure 3. H21 and unilateral gain vs. frequency extrapolated to Ft of 205 GHz and Fmax of 210 GHz.

Peak Ft is reached at a modest 8 mA/μm² and this device is expected to meet performance and power requirements of most 40Gb circuits.

5. Conclusion

SiGe BiCMOS is well poised to meet a large number of requirements for wireless and wire-line communication products. In this paper, we reviewed several SiGe BiCMOS technology nodes available at a pure-play commercial foundry and described how each node has been optimized in performance, features, and cost to address a different segment of the communication market.

Performance of SiGe transistors now exceeds Ft and Fmax of 200 GHz with even higher levels of performance likely in the near future meeting the needs of communication products both for today and the foreseeable future.

REFERENCES

- [1] M. Racanelli et al, 2001 IEDM Tech Dig., p. 336
- [2] P. Ye et al., 2002 RFIC Symposium, p. 329