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Sub 100 nm Gate Technologies for Si/SiGe Buried Channel RF Devices

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1. Introduction

Since many years, Si/SiGe heterostructure field-effect transistors have been investigated. Generally, two different kinds of devices have been realized by several groups: Devices with a strained Si channel at the surface [1] and transistors where the channel is buried and modulation doped [2]. Fig. 1 shows a comparison of the effective mobilities from where the much better performance of devices of the second type can be deduced. In this paper, we report on modulation doped field effect transistors (MODFETs), prepared with two different technologies: The definition of the gate has been realized either by e-beam (1) or by optical lithography (2). In the latter case, a self-aligned replacement gate technique has been used which enables gate lengths below 100 nm.

2. Experimental

The MBE grown layer stacks consist of 9 nm thick tensilely strained Si channels on strain relieved graded SiGe buffers with Ge contents of 40...45%. The quantum wells are double sided doped. Both technologies include dry mesa etching, deposition of 200 nm SiO_2 field oxide and ion implantation for the source and drain contacts. The footprint of the e-beam mushroom gates decreased from L_G = 500 nm to below 100 nm over the last 5 years. In case of the newly developed replacement gate technique, a 500 nm broad polyimide dummy gate is defined by optical lithography using a standard mask aligner. This fin acts as a mask for the contact implantation. L_G is defined during a shrinking step by means of dry etching. Subsequently, the polyimide gate is replaced by evaporated Pt/Ti and electroplated Au. In a final etching step the gate head is defined independently from the foot. Gates with a footprint of 100 nm and an aspect ratio of up to 6:1 have been realized up to now. Details of the two processes are published in [2, 3].

3. Results and discussion

In Fig. 2, the gate length dependence of the intrinsic transconductance g_{mi} is shown. Both technologies can be fitted with one empirical curve indicating the performance improvement by gate scaling. Fig. 3 shows the effect of varying the distance d_{GC} between the channel and the gate for devices realized with technology (2). It is clearly evident that depletion or enhancement characteristics can be adjusted by the epitaxial definition of the layer thicknesses.

Due to the self-alignment, very small G/S and G/D distances can be realized using the replacement gate technique. This results in very high transit frequencies of up to 90 GHz (s. Figs. 4 and 5). On the other hand, the highest maximum frequencies of oscillation f_{max} have been realized up to now with gates prepared by means of e-beam lithography. Fig. 6 shows the gate voltage dependence of f_{max}(U) and f_{max}(MAG) for devices with a gate length of 95 nm, indicating a maximum value of 180 GHz. In this case, the relaxed buffer has been produced by low energy plasma enhanced chemical vapor deposition (LEPECVD) enabling a much higher growth rate and hence a higher throughput than MBE [4]. Comparing the cut-off frequencies achieved with different kinds of devices (s. Fig. 7), buried channel MODFETs show a much better performance than surface channel MOSFETs for all investigated gate lengths due to the above mentioned higher mobility.

The noise behavior of MODFETs has been investigated for frequencies between 2 and 18 GHz. A minimum noise figure F_{min} = 0.3 dB was derived for type (1) devices at 2.4 GHz. A good fit to the measured values can be found using Fukui's empirical model [5]. Putting the equivalent circuit values for type (2) devices into the formulas, even lower noise figures can be estimated (s. Fig. 8).

4. Conclusions

Combining a high rate epitaxy like LEPECVD with the low cost replacement gate technology opens up the capability of SiGe FET device production. Encouraging cut-off frequencies of f_t = 90 GHz and f_{max} = 180 GHz have been shown for buried channel MODFETs.

References

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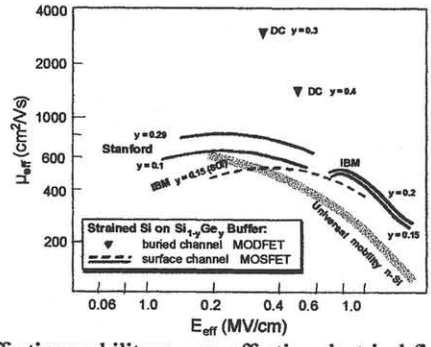

Fig. 1 Effective mobility μ_{eff} vs. effective electrical field E_{eff} of different strained Si channel devices.

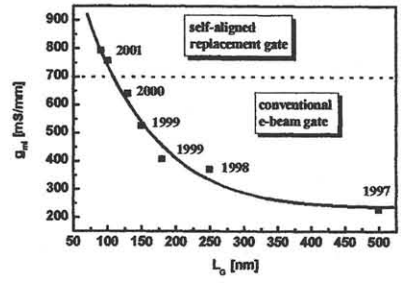

Fig. 2 Gate length dependence of the intrinsic transconductance g_{mi}. The progress is pointed up by the year dates.

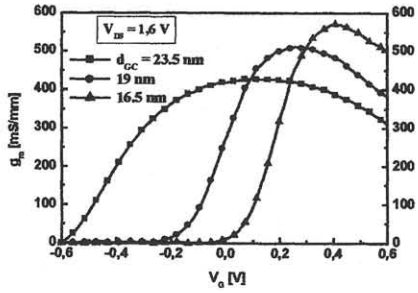

Fig. 3 Transconductance g_m vs. gate voltage V_G of n-MODFETs. Parameter is the gate/channel distance d_{GC}.

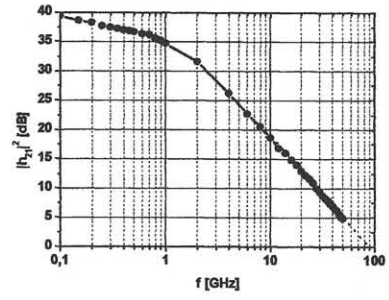

Fig. 4 Current gain $|h_{21}|^2$ vs. frequency of a 100 nm gate length device prepared by the replacement gate technology.

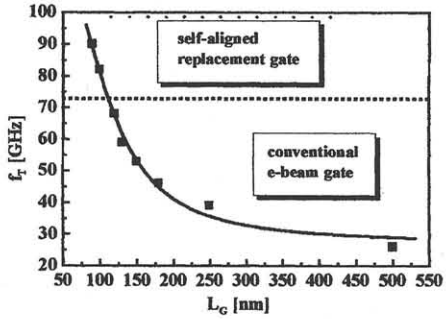

Fig. 5 Transit frequency f_t vs. gate length L_G. Similarly to Fig. 2, both technologies can be fitted with one function.

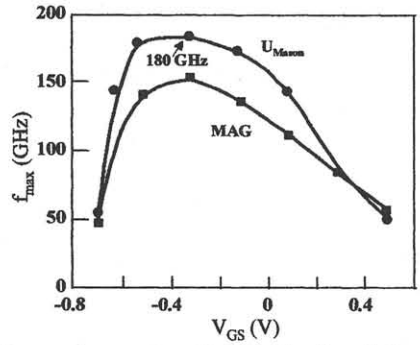

Fig. 6 Maximum frequencies of oscillation f_{max} derived from Mason's gain U and maximum available gain MAG as a function of the gate voltage V_G of an n-MODFET with 95 nm e-beam gates.

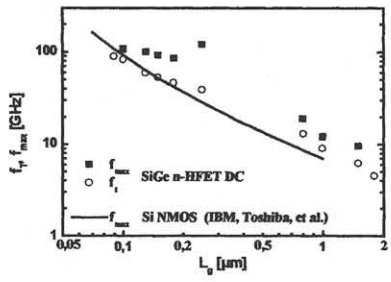

Fig. 7 Comparison of the cut-off frequencies of different technologies as a function of the gate length L_G.

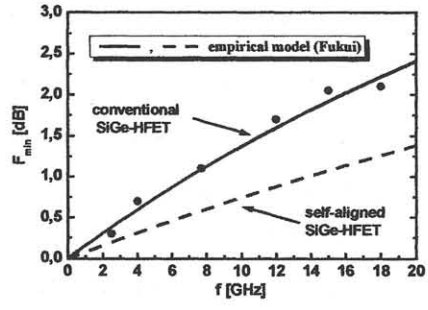

Fig. 8 Frequency dependence of the minimum noise figures F_{min}. (•) measured values, (—) empirical fit after Fukui, (—) estimated model for self-aligned devices.