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Influence of SiGe Channel Position and Fowler-Nordheim Stress on 1/f Noise in SiGe pMOSFETs

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1. Introduction

Beyond the carrier mobility enhancement, the SiGe pMOSFET is expected to have an advantage in 1/f noise [1]. This is conventionally explained by the reduction in either mobility fluctuation ($\Delta\mu$) or carrier number fluctuation (Δn) in the buried channel device [2,3]. The reduction in $\Delta\mu$ is anticipated since the carriers are simply farther away from the scattering sources such as fixed oxide charge and interface roughness [1]. The Δn resulting from the capture/release of carriers involving oxide traps (slow states) near the gate-oxide interface is also considered to be weak in SiGe pMOSFETs since the tunneling probability of carriers from the buried channel to near-interface oxide traps decreases fast as the oxide-to-channel distance ($d_{ox\text{-}ch}$, typically 2-8nm) increases [1]. Furthermore, it has been proposed that the carriers in SiGe pMOSFETs tunnel into a lower density of trap states, responsible for the larger displacement of the hole quasi-Fermi level (E_{FP}) from the valence band edge at the oxide interface (E_{vs}) for the same gate overdrive [4,5]. Nevertheless, it has been reported that the 1/f noise in SiGe pMOSFETs is dominated by Δn rather than $\Delta\mu$ [1,3], suggesting that the oxide trap distribution plays a dominant role in the 1/f noise generation.

Since the Fowler-Nordheim (F-N) stress is conventionally employed to find the relationship between the gate-oxide quality and the 1/f noise in MOSFETs (because it increases the oxide trap density (N_{ot}) significantly) [6,7], it is necessary to examine the 1/f noise in SiGe pMOSFETs under the F-N stress in order to investigate the influence of the channel position and N_{ot} on the 1/f noise behavior in the buried channel device.

2. Device Fabrication and Measurements

The epitaxy by reduced pressure CVD started with a 100Å Si seed, and the growth of a 200Å thick $Si_{0.8}Ge_{0.2}$ channel followed it. Then, a Si-cap layer with three different thicknesses of 60Å (sample I), 80Å (sample II), and 100Å (sample III) was deposited on each wafer. The gate-oxide thickness is 72±2Å for all samples. After the oxidation, the unconsumed Si-cap layer thicknesses of the samples I-III were measured to be 21Å, 47Å, and 64Å in average, respectively. Fig. 1 shows the schematic cross-sectional view of the SiGe pMOSFET. The measured DC parameters of the samples are shown in Table. I.

The F-N stressing was performed by applying a constant gate voltage (V_{gs}) of –8V with drain (V_{ds}) and source voltages of 0V for 120 seconds. The V_{th} shift due to the stress is -0.29±0.02V for all samples. The 1/f noise was measured before and after the F-N stress. The normalized drain current spectral density (S_I/I_d^2) was derived from the fluctuation in V_{ds} at the bias condition of V_{ds}=100±5mV and $V_{gs}=V_{th}$-0.7V.

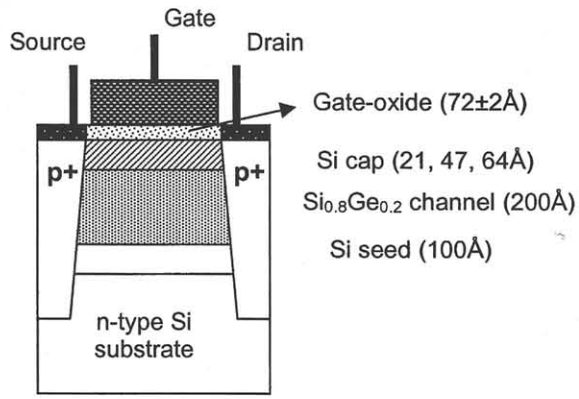

Fig. 1 Schematic cross-sectional view of the SiGe pMOSFET.

Table. I DC parameters of the SiGe and Si pMOSFETs (unstressed) in this work. I_{on}, I_{off} and $G_{m\text{-}max}$ are measured at $V_{ds}=V_{gs}$=-3V, V_{ds}=-3V and V_{gs}=0V, and V_{ds}=-0.1V, respectively.

ID	I_{on} [A/μm]	I_{off} [A/μm]	$G_{m\text{-}max}$ [μS/μm]	V_{th} [V]
I	1.42×10^{-4}	1.39×10^{-11}	10.64	-0.95
II	1.33×10^{-4}	5.99×10^{-12}	9.85	-0.97
III	1.09×10^{-4}	1.07×10^{-11}	9.06	-1.03
Si	1.05×10^{-4}	3.15×10^{-12}	8.87	-1.07

3. Results and Discussion

Fig. 2 (a) and (b) show S_I/I_d^2 vs. frequency of the Si and SiGe pMOSFETs at the given bias condition for before and after the F-N stress, respectively. It is clearly seen that all SiGe pMOSFETs here have significantly lower 1/f noise levels than the Si-control pMOSFET, by an order of 1-2, regardless of F-N stressing, although the noise level elevates after the stress for all samples. This agrees with the presumed fact that the buried channel device is less noisy than the surface channel device as long as the gate-oxide quality is comparable [2], and this is proven to be still valid even after the gate-oxide is degraded by the F-N stress. Meanwhile, it is noted that the noise of SiGe pMOSFETs reveals a dependence on $d_{ox\text{-}ch}$, despite the relatively narrow

$d_{ox\text{-}ch}$ range (21-64Å) used in this study.

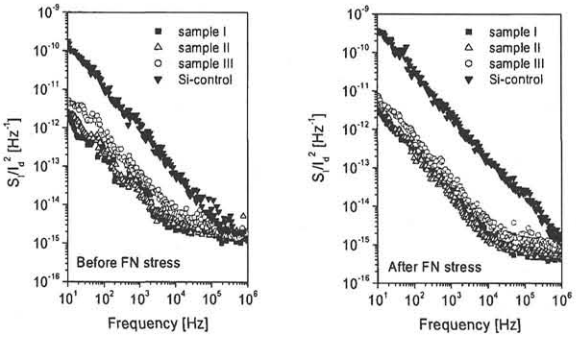

Fig. 2 S_I/I_d^2 vs. frequency for the SiGe pMOSFETs and the Si-control (a) before and (b) after the F-N stress measured at V_{ds}=100±5mV and V_g=V_{th}-0.7V.

Fig. 3 shows the S_I/I_d^2 at 30Hz vs. $d_{ox\text{-}ch}$ for before and after the F-N stress. As illustrated, the minimum 1/f noise occurs at the smallest $d_{ox\text{-}ch}$ of 21Å (sample I) and it does not increase significantly until the $d_{ox\text{-}ch}$ increases up to around 5nm both for before and after the F-N stress. This implies that an around 2nm thick Si-cap is sufficient to suppress the direct tunneling of carriers from the SiGe channel to the oxide traps, but it is found that the further increase in $d_{ox\text{-}ch}$ (especially, when $d_{ox\text{-}ch}$>5nm) only to degrade the 1/f noise characteristics. Since a larger $d_{ox\text{-}ch}$ reduces the tunneling probability significantly, the relatively higher 1/f noise in the SiGe pMOSFET with a $d_{ox\text{-}ch}$ of 64Å (sample III) is considered to be from the parallel channel at the oxide interface rather than from the SiGe buried channel. In turns, it could be said that the parallel channel effect is minimal in the SiGe pMOSFET when the $d_{ox\text{-}ch}$ is less than 5nm, and this coincides with the simulation result [8]. Simultaneously, the 1/f noise in sample III is supposed to be further degraded by the increased N_{ot} near the E_{FP} because it is known that the increase in $d_{ox\text{-}ch}$ reduces the separation between E_{FP} and E_{VS} [5].

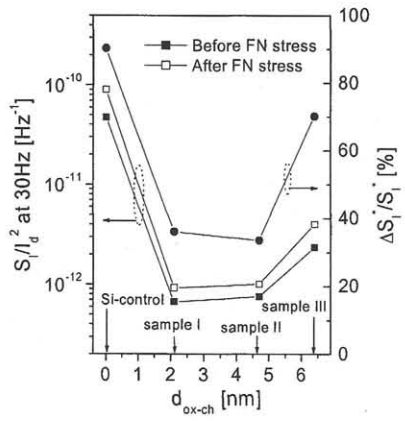

Fig. 3 Dependence of the 1/f noise at 30Hz on $d_{ox\text{-}ch}$ before and after the F-N stress. The % change in S_I/I_d^2 at 30Hz ($\Delta S_I^*/S_I^*$) due to the F-N stress is also shown.

The % change in 1/f noise at 30Hz ($\Delta S_I^*/S_I^*$, where S_I^* is defined as S_I/I_d^2) due to the F-N stress is included in Fig. 3. As seen, the SiGe pMOSFETs with a $d_{ox\text{-}ch}$ of less than 5nm (samples I and II) show a smaller % change in $\Delta S_I^*/S_I^*$ of 34-36% than the SiGe pMOSFET with a $d_{ox\text{-}ch}$ of 64Å (sample III, 70%) and the Si-control (91%). It is suggested that the lower $\Delta S_I^*/S_I^*$ for the samples I and II is attributed to the smaller % change in N_{ot} ($\Delta N_{ot}/N_{ot}$) near the E_{FP} when the separation between E_{FP} and E_{VS} is larger.

N_{ot} at the Fermi level can be extracted from the conventional Δn model equation [3], and the calculated values of the Si-control pMOSFET are $5.2x10^{17}cm^{-3}eV^{-1}$ and $1.2x10^{18}cm^{-3}eV^{-1}$ (i.e. $\Delta N_{ot}/N_{ot}$=131%) for before and after the F-N stress, respectively. Since the equation is only valid for the standard surface channel MOSFET, it is difficult to apply the equation directly to the SiGe buried channel pMOSFETs [3]. However, it has been proposed that the equation is effectively used for the SiGe pMOSFET assuming that the parallel channel formation is negligible (in this case, C_{ox} should be replaced by the gate-to-channel capacitance) [5]. Using the assumption, it is found that the N_{ot} at E_{FP} varies from $7.9x10^{15}cm^{-3}eV^{-1}$ to $1.4x10^{16}cm^{-3}eV^{-1}$ ($\Delta N_{ot}/N_{ot}$=77%) due to the F-N stress for the sample I, and from $7.1x10^{15}cm^{-3}eV^{-1}$ to $1.2x10^{16}cm^{-3}eV^{-1}$ ($\Delta N_{ot}/N_{ot}$=69%) for the sample II. This suggests that both N_{ot} distribution and $\Delta N_{ot}/N_{ot}$ due to F-N stress are non-uniform with respect to the energy level.

4. Conclusion

In conclusion, the SiGe pMOSFET shows a much lower 1/f noise than the standard Si pMOSFET even after the F-N stress. It is found that the position of a channel relative to the gate-oxide interface is a key parameter in determining the device's 1/f noise behavior if the gate-oxide condition is comparable. The minimum 1/f noise occurs when the $d_{ox\text{-}ch}$ is 2-5nm, responsible for the minimum parallel channel effect and the lower N_{ot} near the E_{FP} resulting from the larger separation of E_{FP} from E_{VS}. The smaller % change in 1/f noise against the F-N stress is also observed for the device with a $d_{ox\text{-}ch}$ of 2-5nm, suggesting the non-uniform % change in N_{ot} distribution versus energy level under the F-N stress. This SiGe pMOSFET design is potentially suitable for the applications requiring a low 1/f noise with high stability.

References

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