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InP-based HEMT Technology and ICs for High-Speed Data Communications

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1. Introduction

Next-generation data communication systems require over-40-Gbit/s operation, low-power consumption, and medium-scale integration for their components. High electron mobility transistors (HEMTs) are one of the most promising devices for meeting these requirements. GaAs pseudomorphic HEMTs (p-HEMTs) are best suited for $LiNbO_3$ modulator drivers because they have both a high cutoff frequency, f_T, (more than 90 GHz) and a high breakdown voltage [1]. InP-based HEMTs are attractive for over-40-Gbit/s digital components, such as multiplexers, demultiplexers, and clock and data recovery circuits, because they have an extremely fast electron transport. A reported InP-based HEMT with a gate length of 25 nm [2] has an f_T of 562 GHz, which is the highest yet reported and sufficient for over-160-Gbit/s signal processing. In this paper we describe an InP-based HEMT technology and digital ICs we have developed.

2. InP-based HEMT Technology

A schematic cross-section of our InP-based HEMT is illustrated in Fig. 1 [3]. We form a recess structure and a Ti/Pt/Au gate by using electron-beam lithography. The gate length is 0.13 μm, which is easily manufacturable. Triple-layer Au-plated interconnections reduce the chip area by 20% and enhance circuit performance in comparison with double-layer interconnections. The benzocyclobutene (BCB) films used as an inter-layer dielectric material have a low relative permittivity (ε_r) of 2.8, providing high-propagation-speed microstrip lines and decreasing parasitic capacitances. Metal-insulator-metal (MIM) capacitors and NiCr thin-film resistors are formed on the InP substrate.

The specifications of the InP-based HEMT technology, including DC and RF characteristics, are summarized in Table 1. The maximum g_m of 920 mS/mm and f_T of 175 GHz are large enough for over-40-Gbit/s signal processing, according to the figure-of-merit proposed by Sano et al. [4].

Device matching, especially uniformity of threshold voltage V_{th} is a key to integration. To improve V_{th} uniformity, we introduced an InP etch-stop layer on the InAlAs carrier supply layer, as shown in Fig. 1. This layer provides precise control of the etching depth in forming the recess region and hence minimizes scatter of the V_{th}. As shown in Table 1, a mean value of -0.633 V and a standard deviation of 13 mV were obtained. Assuming that other scattering factors, such as NiCr resistance and the sheet resistance of the epitaxial layers, are negligible, an analysis like that carried out by Maeda et al. [5] predicts that the maximum operating speed of a D-type flip-flop (D-FF) using our high-speed and uniform HEMT exceeds 60 Gbit/s and that digital ICs containing ten thousands of the D-FFs are producible with a yield of more than 70%. The integration scale is sufficiently large to produce digital ICs for over-40-Gbit/s data communications.

3. InP-based HEMT ICs

Using our InP-based HEMT technology, we designed and fabricated several digital ICs to demonstrate its feasibility. The features of the ICs are summarized in Table 2.

4:1 Multiplexer (MUX) [6]

The 4:1 MUX operates at up to 47 Gbit/s in a module. It uses a full-rate clock and re-times serialized data using a D-FF at the final stage. Full-rate-clock operation of the MUX is desirable for long-distance data transmission because it suppresses output jitter and improves signal quality. A microphotograph of the chip is shown in Fig. 2, and eye diagrams at 43 Gbit/s measured on a wafer are shown in Fig. 3.

1:4 Demultiplexer (DEMUX) [7]

The 1:4 DEMUX operates at more than 50 Gbit/s on a wafer. A novel data splitting technique reduces line lengths in the first 1:2 DEMUX block and minimizes data-pattern-dependent jitter caused by signal reflection. Consequently, a wide phase margin of 108° was observed. Jitter included in the input data dominates the phase margin. If we use a less-jitter signal for the input data, the margin will increase to 250°.

2:1 MUX [8]

The 2:1 MUX is the fastest digital IC yet developed [9]. It serializes two-channel parallel data at up to 90 Gbit/s. To achieve this extremely fast operation, we optimized the transmission lines in the selector and introduced an AC-coupled clock buffer with high gain. A

microphotograph of the chip is shown in Fig. 4.

4. Summary

We described our InP-based HEMT technology and three ICs. The high performances of the ICs clearly demonstrate that the speed and uniformity of the InP-based HEMT technology are sufficient for constructing over-40-Gbit/s digital medium-scale ICs.

Acknowledgments

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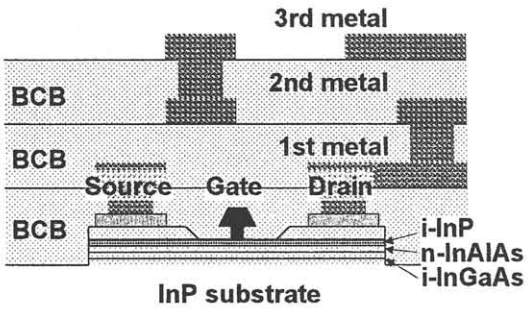

Fig. 1 Cross-section of InP-based HEMT.

Table 1 Specifications of InP-based HEMT technology.

Transistor	InAlAs/InGaAs lattice-matched HEMT
L_g	0.13 μm
g_m	920 mS/mm, σ_{gm}=15 mS/mm @V_{ds}=1 V, V_{gs}=-0.2 V
f_T	175 GHz @V_{ds}=1 V, V_{gs}=-0.2 V
V_{th}	-0.633 V, σ_{Vth}=13 mV
BV_{gdo}	3 V @I_{gs}=0.5 mA/mm
I_{dss}	350 mA/mm
Wire metal	Au, 3 levels
Interlayer	Benzocyclobutene (BCB, ε_r=2.8)
Capacitor	MIM capacitor
Resistor	NiCr, 50 Ω/sheet

Table 2 Features of InP-based HEMT digital ICs.

IC	Bit rate (Gbit/s)	Tr.	Power (W)**	Size (mm)	Ref.
4:1 MUX	47 (Module) 45 (Chip)	1355	7.9	4 x 4.5	[6]
1:4 DEMUX	>50 (Chip)	972	4.7	4 x 3.1	[7]
2:1 MUX	90 (Chip)	210	1.3	1.9 x 1.8	[8]

** Supply voltage: -5.2 V

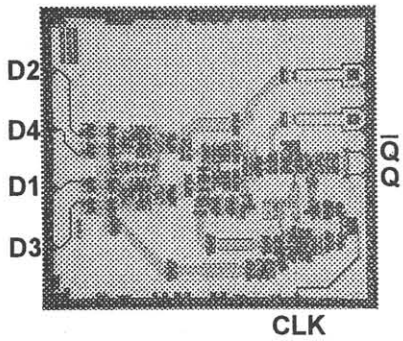

Fig. 2 4:1 MUX IC.

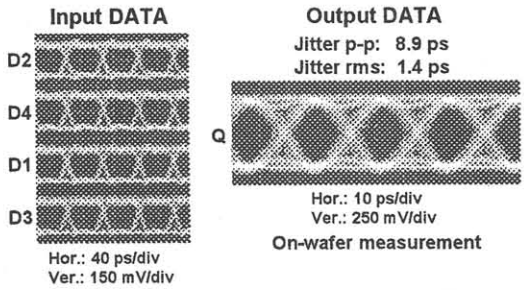

Fig. 3 Eye diagrams at 43 Gbit/s of 4:1 MUX IC.

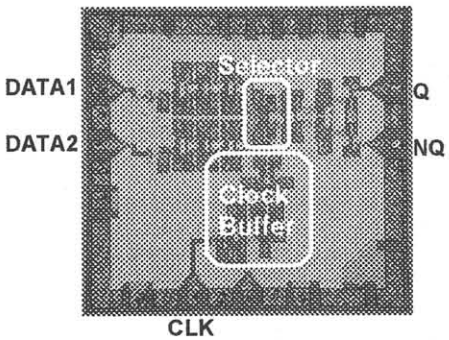

Fig. 4 2:1 MUX IC.