Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 296-297

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Data Limiting-Amplifier, Data Distributor, and Clock Distributor ICs for 40-Gbit/s-class Optical Communication Systems Using InP HEMTs

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1. Introduction

Optical communication systems based on 40-Gbit/s electrical-time-division multiplexing (ETDM) are being developed to offer larger transmission capacity. In the systems, a data limiting-amplifier (DLIM), a data distributor (DDIS), and a clock distributor (CDIS) are important analog circuits. The DLIM outputs the data signal with a constant amplitude over a specified input amplitude range. The DDIS/CDIS distributes a single input data/clock signal to plural functional circuits. To construct these analog circuits, several amplifier sections are connected in series. This circuit configuration increases the gain of the circuit, but it degrades the bandwidth of the circuit. This well-known trade-off between the gain and the bandwidth is a problem even for 40-Gbit/s-class analog circuits, even if the transistors that have state-of-the-art in high-frequency characteristics (e.g. InP HEMTs, InP HBTs) are used. One of the solutions to this problem is to use a circuit configuration that mitigates the trade-off. For example, a 40-Gbit/s DLIM IC with InP HBTs [1] has been realized by using a Cherry-Hooper topology [2] in the amplifiers.

In this paper, we report 40-Gbit/s-class InP HEMT analog ICs including DLIM, DDIS, and CDIS ICs. In order to relax the trade-off between the gain and the bandwidth, several new configurations were investigated. The ICs that was fabricated with the configurations operated at 43 Gbit/s or 43 GHz, which are the bit-rate and the clock frequency of optical channel transport unit 3 (OTU-3) [3] .

2. Circuit Design

Data Limiting-Amplifier (DLIM) IC

Figure 1(a) shows a circuit diagram of the DLIM IC. Its input port is capable of handling both a single-ended and a differential signal. Output signal becomes differential without regard to input signal type. The DLIM IC consists of five sections; an input source follower (ISF), three capacitive-feedback and inductor-peaking amplifiers (CF-IP Amps), and a 50-Ω driver. The ISF, together with on-chip 50-Ω termination resistors, is used as the input interface. For the ISF as well as the source followers in the CF-IP Amps, peaking capacitors are added to compensate for the loss of the gain at high frequency. The CF-IP Amp is a differential amplifier that has two features; 1) the feedback capacitors realized by drain-source-shortened HEMTs and 2) the peaking inductors connected to the load resistors in series. The feedback capacitors [4] decrease the amplifier's input capacitances that the preceding section drives. The peaking inductors decrease the load capacitances that the differential amplifier itself drives. Since the capacitances of different part are cut down, wider extension of the bandwidth is achievable compared to an amplifier that has one of the two features. Simulation predicted that the DLIM with the CF-IP Amps was 95 %, 22 %, and 54 % wider in the bandwidth than a DLIM without the two features, with only the feedback capacitors, and with only the peaking inductors, respectively. The 50-Ω driver is a conventional differential amplifier whose output is open-drain type.

Data Distributor (DDIS) IC

Figure 1(b) is a circuit diagram of the DDIS IC. A single-ended data signal is input, and outputs are two pairs of differential

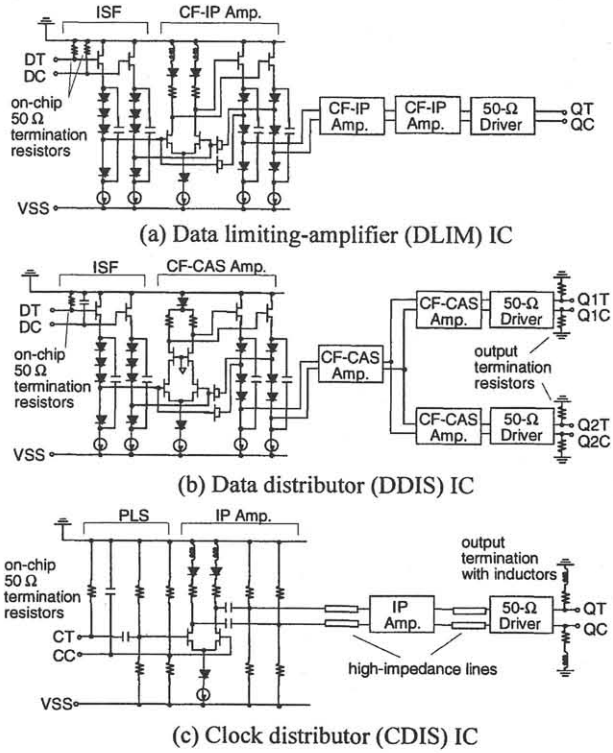

Figure 1. Circuit diagrams of the data limiting-amplifier, the data distributor, the clock distributor ICs.

data signals, in other words, there are four single-ended output data signals (two of them inverted). The IC comprises an ISF, four capacitive-feedback and cascode amplifiers (CF-CAS Amps), and two 50-Ω drivers. The ISF is identical to that in the DLIM IC. The CF-CAS Amp simultaneously uses the feedback capacitors and the cascode configuration. As described in the DLIM IC design, the feedback capacitors reduce the input capacitances of the amplifier. The cascode configuration mitigates the Miller effect, so that the input capacitances of the amplifier decrease further. With these features, the bandwidth of the DDIS IC expands. Simulations indicated that the DDIS with the CF-CAS Amps was 117 %, 40 %, and 66 % wider in the bandwidth than a DDIS without the two features, with only the feedback capacitors, and with only the cascode configuration, respectively. The 50-Ω drivers are the same as those in the DLIM IC, except that the output termination resistors are added to avoid reflections at the IC output node.

Clock Distributor (CDIS) IC

Figure 1(c) shows a circuit diagram of the CDIS IC. Input is a single-ended clock, and outputs are differential clocks. Then, two single-ended clocks, which differ in phase by 180°, can be obtained from a single-ended clock input. The IC has four blocks, which are the passive level shifter (PLS), two inductor-peaking amplifiers (IP Amps), and the 50-Ω driver. The PLS and the IP Amps are almost the same as those in [5]. The 50-Ω driver is also identical to that in the DLIM and the DDIS ICs. To increase the gain at over 40 GHz, we devised two points;

1) output terminations with inductors and 2) high-impedance lines that interconnect the blocks. The output termination with inductors causes gain peaking at high frequency. The high-impedance lines are generally inductive, so that they effectively act as inductors and, together with the input capacitances of the IP Amps, cause gain peaking. With these two techniques, 2.7-dB gain increase at 43 GHz, to which the output termination with inductors and the high-impedance lines contribute 1.6 dB and 1.1 dB respectively, is expected by simulation.

3. Fabrication

The ICs were fabricated with 0.1-μm InP HEMTs [6]. The transconductance (g_m), current cut-off frequency (f_T), threshold voltage (V_{th}), and standard deviation of V_{th} are typically 1.1 S/mm, 168 GHz, -0.58 V, and 40 mV, respectively. All chips are 2 x 2 mm².

4. Experimental Results

All the ICs were measured on-wafer with RF probes. For the DLIM and DDIS ICs, a 43-Gbit/s single-ended data signal was input. The data signal was 2^{31}-1 pseudo-random-bit-streams (PRBSs) generated by the combination of a four-channel pulse pattern generator, a 4:2 multiplexer unit, and an InP HEMT 2:1 selector module [7]. For the CDIS IC, a 43-GHz single-ended clock signal generated in a synthesizer was input. All output waveforms were monitored by a sampling-oscilloscope.

Data Limiting-Amplifier (DLIM) IC

Figure 2 shows 43-Gbit/s operating waveforms for two inputs that differ in amplitude. Figure 2(a) shows the operating waveforms for the input of 964-mV_{pp} peak-to-peak and 545-mV_{pp} eye-openings, and Figure 2(b) shows those for the input of 159-mV_{pp} peak-to-peak and 78-mV_{pp} eye-openings. Though there were 16-dB differences between the two inputs, the IC output clear eye-openings for both the inputs. Also, for the input of over ~200-mV_{pp} eye-openings, output eye-opening saturation with over 700-mV_{pp} was confirmed. We also evaluated the root-mean-square (RMS) jitter at the cross point in the eye waveforms. The RMS jitter increases due to the DLIM IC were relatively low of 0.19 ps (input: 1.30 ps; output: 1.49 ps) and 0.28 ps (input: 1.38 ps; output 1.66 ps) for the operation conditions shown in Figure 2(a) and (b), respectively. The power consumption was 0.54 W at supply voltage of -4.5 V.

Data Distributor (DDIS) IC

Figure 3 shows operating waveforms at 43 Gbit/s. Two of four outputs (Q1T, Q2T) were monitored while the other two outputs (Q1C, Q2C) were terminated with 50-Ω resistors outside the IC. An 813-mV_{pp} input data signal was successfully distributed to the output nodes with clear eye-openings and over 1100-mV_{pp} amplitudes. Also, for the 570-mVpp input (3-dB less than the input under the operating condition in the Figure 3), outputs almost the same as shown in Figure 3 were obtained. The RMS jitter increase by the DDIS IC was about 0.3 ps (input: 1.5 ps; output 1.8 ps). The power consumption was 1.74 W at supply voltage of -5.2 V.

Clock Distributor (CDIS) IC

Figure 4 shows operating waveforms for a 43-GHz 1000-mV_{pp} clock input signal. In this measurement, the output clock signals were derived through the 50-cm semi-rigid cables that had ~2.5-dB loss at 40 GHz. Nonetheless, the IC output two 43-GHz over-900-mV_{pp} clock signals at the sampling-oscilloscope inputs. The operation frequency range was also measured for the 1000-mV_{pp} input. From 2 to 47 GHz, two output clock signals with over-800-mV_{pp} were obtained. The power consumption was 0.51 W at supply voltage of -5.2 V

5. Conclusion

We have described 40-Gbit/s-class InP HEMT analog ICs including a data limiting amplifier IC, a data distributor IC, and a clock distributor IC. In order to relax the trade-off between the gain and the bandwidth in the differential amplifiers, several new circuit configurations were investigated. The ICs fabricated with the new configurations were confirmed to operate at 43 Gbit/s or 43 GHz, which are the bit-rate and the clock frequency of OTU-3.

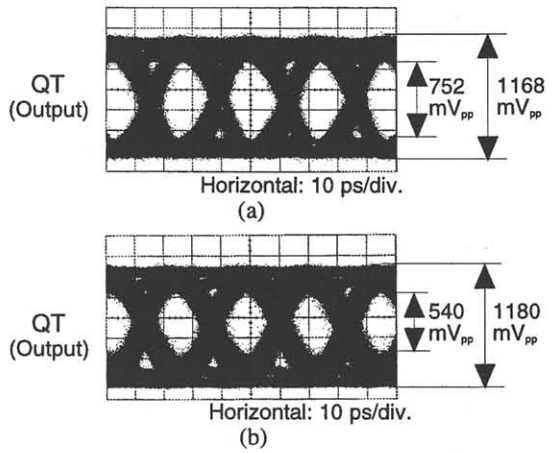

Figure 2. Operating waveforms of the data limiting-amplifier IC at 43 Gbit/s.
(a) : Input of 964-mV_{pp} peak-to-peak and 545- mV_{pp} eye-openings
(b): Input of 159-mV_{pp} peak-to-peak and 78-mV_{pp} eye-openings

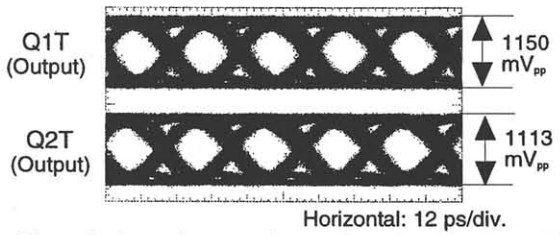

Figure 3. Operating waveforms of the data distributor IC for a 43-Gbit/s 813-mV_{pp} single-ended data input.

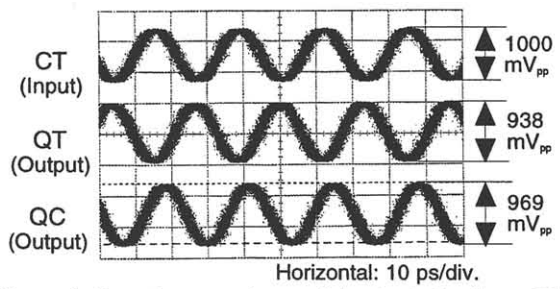

Figure 4. Operating waveforms of the clock distributor IC at 43 GHz.

Acknowledgements

The authors thank H. Tomiyama for his measurement assistance, and E. Sano, H. Toba, Y. Yamane, and M. Muraguchi for their encouragement throughout this work.

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