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Double-recessed 0.1-μm-gate InP HEMTs for 40-Gb/s Optical Communication Systems

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1. Introduction

InP HEMTs are promising for ultra-high-speed ICs using in 40-Gb/s optical fiber communication systems because of their superior high frequency performances, and the f_T over 400 GHz has been already achieved [1]. However, as reducing the gate length down to 0.1-μm-region to improve the device performance, the electric field strength under the gate area becomes high, which induces serious increase of the drain conductance (g_d) and reduction of the breakdown voltage (BV_{ds}) due to a large impact ionization ratio of the narrow band-gap $In_{0.53}Ga_{0.47}As$ channel [2,3]. In order to improve the g_d and the BV_{ds} maintaining the high-speed device performance, we have developed the double-recessed 0.1-μm-gate InP HEMTs and have successfully achieved the high-speed SCFL (Source-Coupled FET Logic) circuit operation.

2. Double-recessed-gate InP HEMT Structure

Figure 1 shows the cross-sectional structures of the double-recessed-gate InP HEMT (DR-HEMT) and the conventional single-recessed-gate InP HEMT (SR-HEMT) used in this study. All the layers were grown by MBE on 3-inch InP-substrates. Both devices have the identical epitaxitial layers under the gate rigions. As for the cap layers, SR-HEMT uses the single n^+-InGaAs ohmic contact layer while DR-HEMT uses the multi-layer structure, which consists of u-InGaAs spacing, n^+-InAlAs etch-stop and n^+-InGaAs ohmic contact layers.

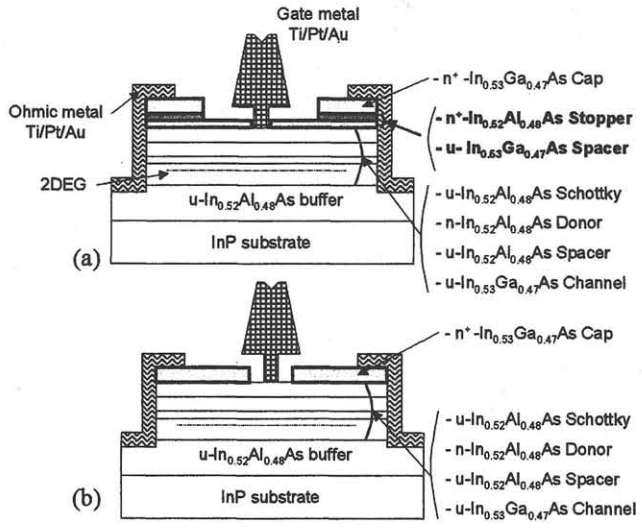

Fig. 1 Schematic cross-sections of the (a) DR- and (b) SR-HEMTs

The gate recesses were formed by selective wet etching of InGaAs/InAlAs using citric acid solution. Introduction of the u-InGaAs spacing and the n^+-InAlAs etch-stop layers can precisely control both the outer and the inner recessed depths for DR-HEMT, which leads to good uniformity of device characteristics such as transconductance (g_m) and threshold voltage (V_{th}). The recess widths were 0.2-μm for SR-HEMT, and 0.8-μm/0.12-μm for outer/inner recesses in DR-HEMT, respectively. After the 0.1-μm T-shaped Ti/Pt/Au gate was formed, all the devices were fully passivated by 600-nm-thick SiN films.

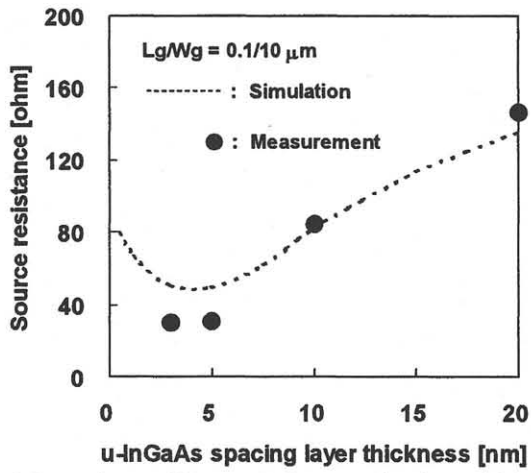

Fig. 2 Dependence of R_s on u-InGaAs spacing layer thickness

Under the ohmic region in DR-HEMT shown in fig. 1, there exist two hetero-barriers: n^+-InGaAs/n^+-InAlAs and u-InGaAs/u-InAlAs interfaces, which strongly affect the source resistance (R_s) of the device. In order to suppress the influence of the hetero-barriers, the thickness of u-InGaAs spacing layer was optimized with respect to the R_s. The dotted line in fig. 2 shows the simulated R_s as a function of u-InGaAs spacing layer thickness. The simulation was performed taking into account of the tunneling current component through the hetero-interface and the series resistance under the outer recessed region. As shown in fig. 2, there is an optimum thickness for u-InGaAs spacing layer at around 3-5 nm. When the u-InGaAs spacing layer is too thick, two-dimensional electron gases are formed in there, thus the electron concentration in the channel region decreases.

Therefore, the R_s increases due to a reduction of the tunneling current to the channel region. On the other hand, when the u-InGaAs spacing layer thickness is too thin, the series resistance under the outer recessed region increases due to the surface depletion, thus the R_s increases again. The measured R_s shown in fig. 2 agree well with the simulated curve. The minimum R_s of as low as 0.30-ohm·mm for DR-HEMT was obtained at the u-InGaAs spacing layer thickness of 3 nm, which was almost comparable with that of 0.26-ohm·mm for SR-HEMT.

3. Device characteristics

Figure 3 shows the typical I-V characteristics for DR- and SR-HEMTs. The V_{th} of both devices were -551 mV and -510 mV, respectively. A good saturation characteristic with smaller g_d and larger BV_{ds} was obtained for DR-HEMT. Table I summarizes a comparison of DC and RF characteristics for DR- and SR-HEMTs. Although the g_m and the f_T were slightly lower for DR-HEMT compared with SR-HEMT, larger g_m/g_d gain and f_{max} were obtained due to the smaller g_d.

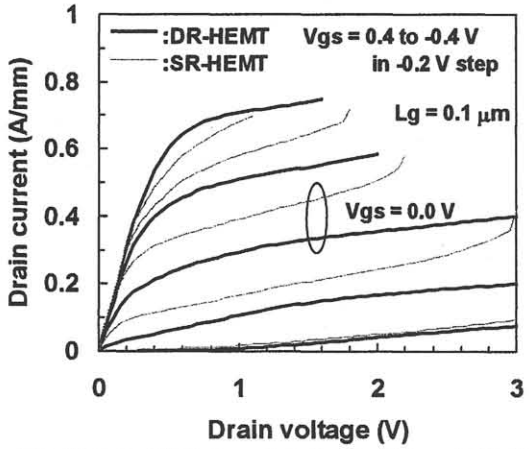

Fig. 3 Typical I-V characteristics for DR- and SR-HEMTs

Table I Characteristics of DR- and SR HEMTs

	g_m [mS/mm]	g_d [mS/mm]	g_m/g_d	f_T [GHz]	f_{max} [GHz]
DR-HEMT	1170	45	26	210	351
SR-HEMT	1370	122	11	233	275

4. Application to 40-Gb/s digital circuit

The 29-stage SCFL ring-oscillators implemented by DR- and SR-HEMTs were fabricated to evaluate the high-speed device performances for digital circuit application. The propagation delay (t_{pd}) of a SCFL inverter was 5.8 ps/gate for DR-HEMT, while it was 6.5 ps/gate for SR-HEMT. The standard deviation of t_{pd} (σt_{pd}) for DR-HEMT was as small as 0.05 ps/gate within a 3-inch wafer, which was resulted from the good uniformity of the inner and the outer recessed profiles by introducing the etch-stop layer. The improvement in t_{pd} for DR-HEMT is believed to be due to the higher g_m/g_d gain compared with SR-HEMT.

We applied the DR-HEMT to a static 1/2-frequency divider IC consisting of a toggle flip-flop and buffers based on SCFL. Figure 4 shows the maximum operation frequencies ($f_{op\text{-}max}$) as a function of g_d. As shown in fig. 4, the $f_{op\text{-}max}$ strongly depends on g_d. By using DR-HEMT with small g_d, stable operations over 40-GHz have been successfully achieved. The maximum value of $f_{op\text{-}max}$ was 43-GHz for DR-HEMT, while it was 38-GHz for SR-HEMT. This result clearly suggests that not only the improvement of g_m or f_T but the suppression of g_d is quite important to achieve a stable high-speed operation of InP-based IC.

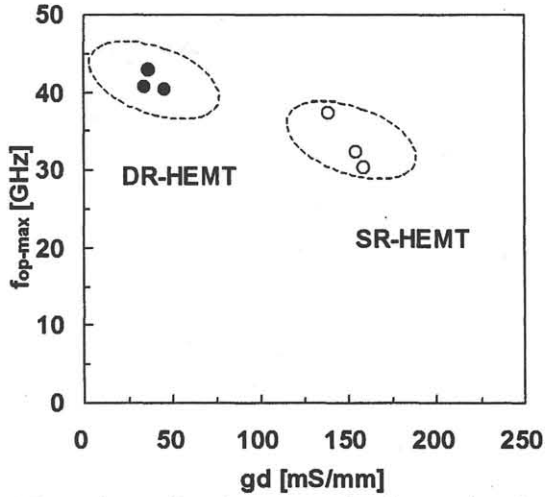

Fig. 4 Dependence of maximum operation frequencies of static 1/2 frequency divider ICs on g_d for DR- and SR-HEMTs

5. Conclusions

We have developed the double-recessed 0.1-μm-gate InP HEMT. It was found that the R_s of the DR-HEMT was strongly affected by the u-InGaAs spacing layer thickness. By optimizing the u-InGaAs thickness, we obtained the minimum R_s of 0.30-ohm·mm. The DR-HEMT showed the improved g_m/g_d gain and f_{max} compared with the SR-HEMT, because of the reduction of g_d. The t_{pd} of SCFL inverter implemented by the DR-HEMT was as fast as 5.8 ps/gate with good uniformity of 0.05 ps/gate. Then, we applied the DR-HEMT to a static 1/2-frequency divider and obtained a stable operation up to 43-GHz. We have confirmed that the double-recessed 0.1-μm-gate InP HEMT is promising for 40-Gb/s optical fiber communication systems.

References

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