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2.2 W/mm GaAs HFET with Field-Modulating Plate Operated at 32 V

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1. Introduction

In modern wireless-communication systems, a high output power amplifier with low distortion and high efficiency is strongly demanded for cellular base station applications. Higher voltage operation is one of the most desirable solutions for these requirements. In order to develop a device operable at higher voltages, we have been investigating a GaAs-based heterostructure FET (HFET) with a field-modulating plate (FP-HFET)[1-3].

In this paper, we describe the optimization of FP length of the FP-HFET with a newly developed overhanging gate structure. The fabricated FP-HFET demonstrated a record high output power density with a high efficiency under high voltage operation.

2. Device fabrication and DC performance

Figure 1 shows the cross-sectional view of the developed FP-HFET with an overhanging configuration. The eaves of the T-shaped WSi/Au gate, which overhangs on the surface passivation film toward the drain electrode, function as an FP electrode. The adoption of the overhanging structure enables reducing the FP formation step in the FP-FET processing reported previously[1-3]. The HFET consists of a Si-doped AlGaAs Schottky layer and a Si-doped GaAs channel layer. The gate length (L_g) was 1.0 μm and the recess length between gate and the recess edge at the drain side (L_{gdr}) was 2.5 μm. The FP length (L_f) was varied from 0.4 μm to 2.5 μm.

The fabricated FP-HFET exhibited a maximum drain current (I_{max}) of 330 mA/mm and a threshold voltage of −2.8 V. Figure 2 shows the drain current pulse dispersion characteristics under pulsed operation for the device with an FP length of (a) L_f = 0.4 μm and (b) L_f = 1.0 μm respectively. The gate was driven from −3.2 V to +1.0 V with a pulse width between 10 μsec and 100 msec, and the drain current was measured while the FET was turned on (V_g = +1.0 V). The device with a short FP (L_f = 0.4 μm) showed significant drain current pulse dispersion as shown in Fig. 2(a). However, the dispersion becomes smaller as the FP length is longer. The device with an FP length of 1.0 μm exibited negligible dispersion as shown in Fig. 2(b). These results indidate that the introduction of the adequately long FP more than 1.0 μm suppresses the channel constriction effect caused by surface trapped charge, thus enabling large drain current swing during large signal RF operation[1].

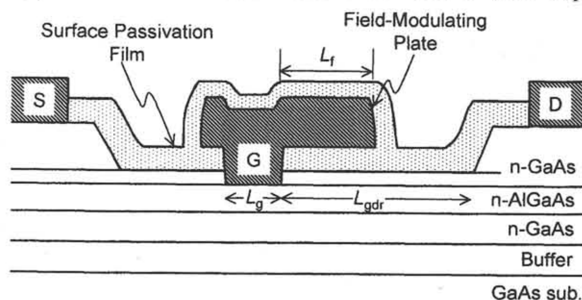

Fig. 1 Schematic cross-sectional view of the developed FP-HFET.

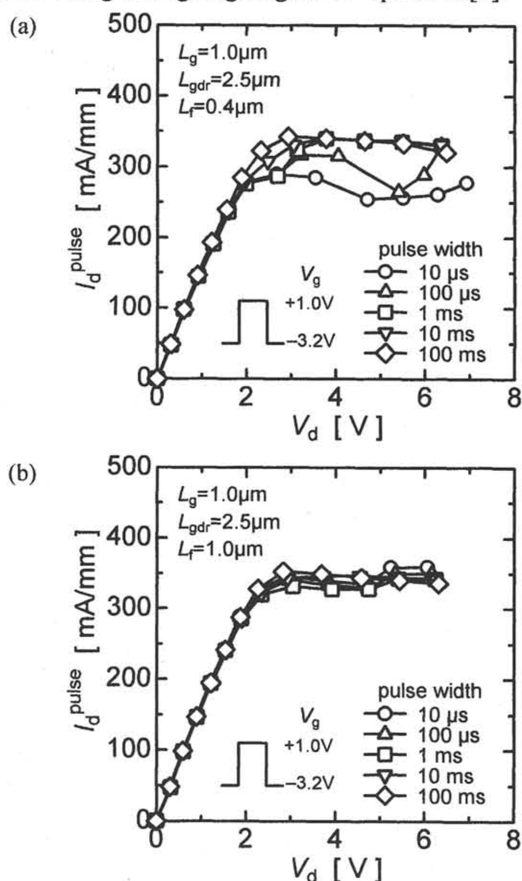

Fig. 2 Pulse *I-V* characteristics for the device with the FP length of (a) L_f = 0.4 μm and (b) L_f = 1.0 μm respectively.

Figure 3 shows the FP length (L_f) dependence of the three-terminal off-state breakdown voltage (BV_3) defined at I_d = 1 mA/mm. The drain current injection technique[4] was employed for the BV_3 measurement. BV_3 is almost unchanged in the FP length range from 0.4 μm to 1.5 μm.

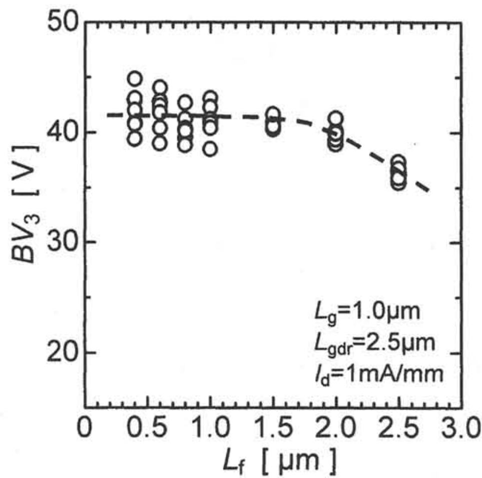

Fig. 3 The FP length (L_f) dependence of the three-terminal off-state breakdown voltage (BV_3).

On the other hand, the FP longer than 1.5 μm gradually reduces the BV_3 since the electric field at the FP edge is increased as the FP edge approaches the drain edge. We thus conclude that the FP length (L_f) should be less than 1.5 μm for the high-voltage device operation.

3. RF performance

RF power performance was evaluated at 1.95 GHz under various drain bias voltages with a drain bias current (I_{dset}) of 6% I_{dss} (class AB). The device had a total gate width (W_g) of 2.64 mm with a unit gate width of 220 μm. Figure 4 shows the drain bias voltage (V_d) dependence of the output power density for the devices with various FP length. The device with an FP length of 1.0 μm exhibited a linear increase in the output power up to 32 V. When the FP length is shorter or longer than 1.0 μm, the increase rate of the output power degraded at V_d values more than 20 V and 25 V respectively. The former is because drain current swing is limited by the channel constriction effect as shown in Fig. 2(a). The latter is because drain voltage swing is limited by the breakdown voltage as shown in Fig. 3.

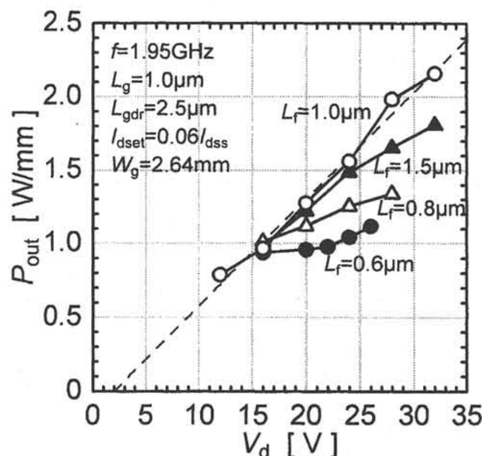

Fig. 4 Drain bias voltage (V_d) dependence of the output power density for the devices with various FP length.

Figure 5 shows the output power (P_{out}) and power-added efficiency (PAE) of the device with a 1.0 μm-long FP as a function of the input power (P_{in}) at V_d = 32 V. The maximum output power of 5.8 W, indicating the power density of 2.2 W/mm, was obtained with a high linear gain of 14.5 dB and a high PAE of 67%. To our knowlege, this is the highest output power density in the GaAs-based FET[1].

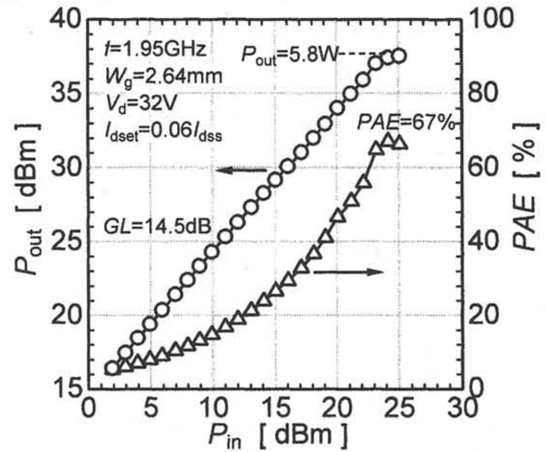

Fig. 5 Output power (P_{out}) and power-added efficiency (PAE) versus input power (P_{in}) at 1.95 GHz and V_d = 32 V for the FP-FET with a 1.0 μm-long FP.

4. Conclusions

We have newly developed a GaAs-based FP-HFET with an overhanging configuration. Due to the optimization of the FP length in terms of both suppressing the channel constriction effect and achieving a high breakdown voltage, the device demonstrated a 2.2 W/mm output power density with a linear gain of 14.5 dB and a power-added efficiency of 67% at 32 V operation. These results indicate that the FP-HFET is promising as a high-voltage operation power device for high power solid state amplifier applications.

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