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60-GHz Single-chip Receiver 3-D MMIC using Commercial GaAs pHEMT Technology

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1. Introduction

The strong demand for high-speed wireless applications has stimulated the development of low cost and compact millimeter-wave wireless equipment. V-band wireless systems are very interesting since they offer much higher transmission rates due to their wide bandwidths. MMICs are the key components and are suitable for realizing cost-effective and compact V-band wireless equipment. Reported V-band receivers were constructed from individual MMIC building block components, the so-called multi-chip configuration[1], [2]. In the millimeter-wave range, interactions between individual MMICs are difficult to control due to the need to set multiple interconnections by using wire-bonding or flip-chip technology. Therefore, a single-chip configuration that integrates all core elements is attractive for improving the performance and for reducing assembly costs. However, the V-band single-chip receiver MMIC reported by Zelly[3] was quite big (5.8 mm x 2.2 mm) and did not integrate the LO elements, resulting in millimeter-wave interconnections and high cost.

Authors have proposed and demonstrated the three-dimensional (3-D) MMIC technology[4], which can greatly reduce circuit area. It offers high-level integration on a single-chip, resulting in compact MMICs and a significant reduction in millimeter-wave packaging cost.

This paper presents a newly developed fully monolithic 60-GHz single-chip receiver 3-D MMIC. The MMIC was fabricated by combining a commercial 0.15 μm GaAs pHEMT technology with the 3-D MMIC interconnection technology[4]. This fabrication methodology can realize compact, high-level integration, and high performance V-band MMICs.

2. Fabrication process

Fig. 1 illustrates the structure of the 3-D MMIC combined with a commercial foundry device. We combined a commercial 0.15 μm GaAs pHEMT foundry process (UMS PH15[5]) from United Monolithic Semiconductor S.A.S. (UMS) with the 3-D MMIC interconnection process from NTT Electronics Corp. (NEL) that originated in NTT Laboratories[6]. The 3-D interconnection layer, which consists of four layers of 2.5-μm-thick polyimide film and 1-μm-thick metal (2-μm-thick for the top metal), was formed on the top layer of the PH15 process. Fig. 2 shows the simple development flow. After designing and drawing MMICs, generated mask data is divided to the device process data and the interconnection process data. Next, the device process is performed and fabricated wafers are delivered to an interconnection foundry. After evaluating device performance, the interconnection layers are formed on the wafers. Design and layout can be modified by using real device parameters that are measured, if necessary. The final pHEMT performance after the 3-D MMIC process achieves an f_T of 110 GHz and an f_{max} of 170 GHz despite the increase in parasitic capacitance around the transistor due to the formed polyimide film.

3. Receiver design and performance

A block diagram of a single-chip receiver MMIC is shown in Fig. 3. The receiver consists of a two-stage LNA, a single-ended drain mixer associated with an IF amplifier, a harmonic oscillator with an active load, a balanced frequency doubler supported by input and output amplifiers, and an amplifier that outputs a signal to a PLL.

The first LNA consists of two 2 x 50 μm gate width pHEMT devices and low-loss matching circuits. The TFMS line with ground slit[7] reduces the loss of the matching circuits, resulting in 12 dB gain and less than 3.5 dB noise figure. The second LNA employs cascode-connected pHEMT devices. This configuration realizes both high gain and compact circuit size; the amplifier gain can be effectively controlled through the second gate bias of the cascode devices. The harmonic oscillator employs a series feedback configuration, a varactor, and an active load. The active load, which consists of a common-gate pHEMT device, offers a low-load impedance over a wide frequency range. The fundamental and second harmonic signals are divided and filtered within the active load. The fundamental signal is fed to an output port for PLL loop input via an associated amplifier; the second harmonic signal is fed to the frequency doubler. The balanced frequency doubler consists of two pHEMT devices, compensated Marchand balun[8], and matching circuits. Supported Ka-band and V-band amplifiers are integrated with the doubler. The LO signal power level from the LO part exceeds -5 dBm. Each element selectively uses the ground plane on the middle polyimide layer to realize a stacked configuration, resulting in compactness (see Fig. 4).

Fig. 4 shows a photograph of the fabricated V-band single-chip receiver MMIC. The chip is just 2.1 mm x 2.4 mm. All elements are present on the fabricated chip and interaction is negligible. Fig. 5 demonstrates the measured conversion gain of the receiver MMIC. The conversion gain exceeds 36 dB in the RF frequency range of 59 GHz to 61.5 GHz. The associated noise figure is less than 5.5 dB over the measured frequency range shown in Fig. 5. The oscillation frequency of the harmonic VCO was tuned to generate an IF frequency of 1 GHz according to RF frequencies. The supplied drain biases are 5 V (for the second LNA and the IF amplifier) and 2.5 V (for the other elements). The power consumption is 1.1 W.

4. Conclusions

This paper demonstrated a fully monolithic 60-GHz single-chip receiver 3-D MMIC using a commercial GaAs pHEMT foundry device. The MMIC achieves 36 dB conversion gain and less than 5.5 dB noise figure. These results indicate that the 3-D MMIC technology combined with commercial foundry device technology promises compact, highly-integrated, and low-cost V-band MMICs and wireless equipment.

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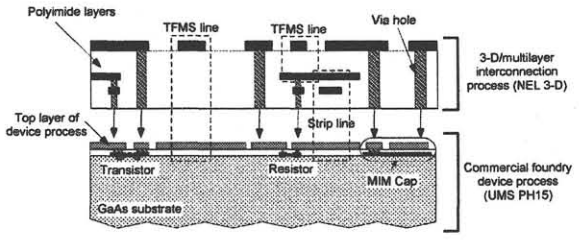

Fig. 1 Structure of 3-D MMIC fabricated by combining commercial foundry process with 3-D MMIC interconnection process.

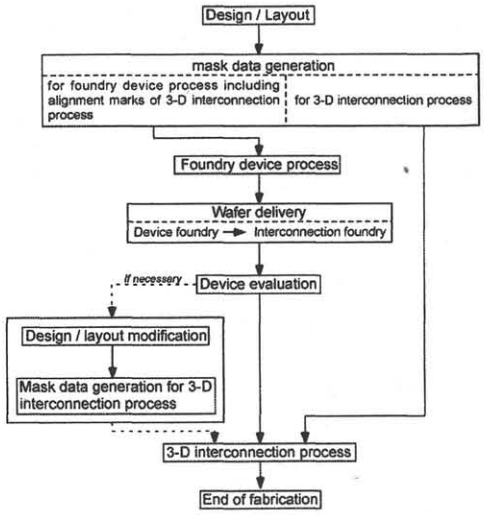

Fig. 2 Development flow of 3-D MMIC

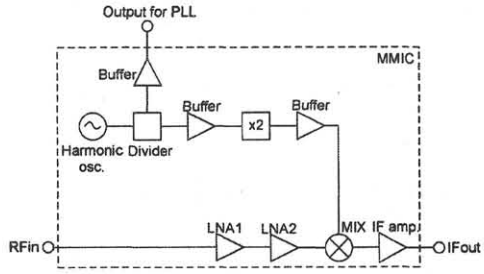

Fig. 3 Block diagram of single-chip receiver 3-D MMIC.

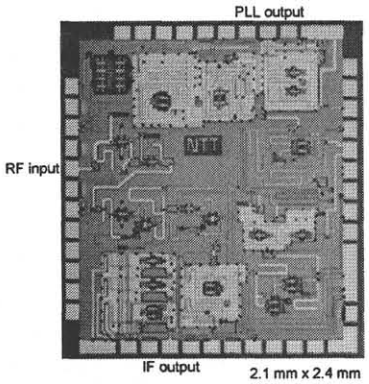

Fig. 4 Photograph of single-chip receiver 3-D MMIC.

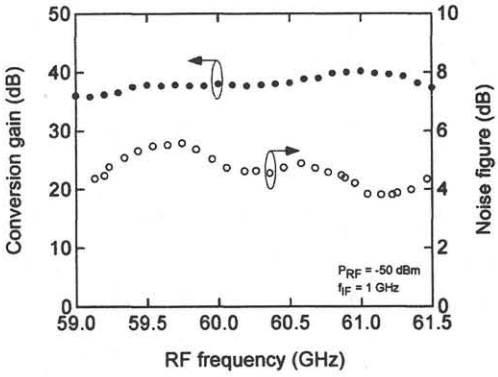

Fig. 5 Measured performance of fabricated receiver 3-D MMIC.