Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 108-109

F-2-5

Tunneling Barrier Structure in Room-Temperature Operating Silicon Single-Electron and Single-Hole Transistors

M. Saitoh, H. Majima, and T. Hiramoto

Institute of Industrial Science, University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
Tel: +81-3-5452-6264, Fax: +81-3-5452-6265, e-mail: masumi@nano.iis.u-tokyo.ac.jp

1. Introduction

Fabrication techniques for high-temperature operating silicon single-electron transistors have been developed by many groups. In order to obtain much clearer Coulomb blockade oscillations at room temperature (RT), it is essential to clarify the formation mechanism of the dots and the tunneling barriers. We have reported that the quantum confinement effects would be a possible origin for the barriers [1]. Shiraishi et al. [2] and Horiguchi et al. [3] discussed the compressive strain during thermal oxidation for a possible origin of the potential well. However, the formation mechanism of the dots and the tunneling barriers has not been completely clarified yet.

In this paper, we investigate the tunneling barrier structure formed in the RT operating silicon single-electron transistors and single-hole transistors. Coulomb blockade characteristics of both electrons and holes in the same channel are studied by using a special device configuration. It is found that the valence band has higher tunneling barriers and smaller dots (potential wells) than the conduction band.

2. Fabrication

The device configuration is similar to the devices in Ref. [1] and has both n- and p-type source/drain contacts. In this study, the device is an ultra-narrow channel MOSFET instead of a point-contact channel MOSFET. While the devices in Ref. [1] showed Coulomb blockade oscillations only at low temperatures, the devices fabricated in this study operate as single-electron transistors and single-hole transistors even at RT because the formed channel is extremely narrow. Figure 1 shows a top schematic view of the fabricated n- and p-type ultra-narrow channel MOSFET [4]. The ultra-narrow channel is formed by EB lithography, reactive ion etching, and isotropic wet etching using SC1 ($NH_4OH/H_2O_2/H_2O$). 14-nm-thick gate oxide is formed by thermal oxidation and poly-Si gate is deposited by LP-CVD. The final channel width is typically less than 5 nm. When positive V_g is applied, electrons are induced in the channel, and when negative V_g is applied, holes are induced in the same channel. This device structure enables the investigation into the transport properties of both electrons and holes in the same physical channel profile.

3. Measurement

Figure 2 shows the typical I_d - V_g characteristics in the fabricated n- and p- type ultra-narrow channel MOSFETs at RT. Coulomb blockade oscillations are observed in both the n- and p-type regions in each sample. This is one of the clearest RT observations of Coulomb blockade oscillations in single-hole transistors that have ever been reported.

Figure 3 shows the I_d - V_g characteristics in the ultra-narrow channel MOSFETs at 50 K. Irregular current peaks are observed in both the n- and p-type regions. This means that serially coupled dots are naturally formed in the valence band as well as in the conduction band. In the n-type region, the current increases more rapidly with increasing the gate voltage. This indicates that the tunneling barriers formed in the conduction band are lower than the valence band. Moreover, the peak-to-valley current ratio of Coulomb blockade oscillations in the p-type region is higher than the n-type region as a whole. More detailed data of Sample A and C are shown in Figs. 4 and 5. In Fig. 4, the peak-to-valley current ratios of the oscillations in both regions are comparable, although the measurement temperature for the n-type region is twice as high. Also, the current peak spacing in the p-type region is about three times as large as the n-type region. The same feature is also observed in Fig. 5. It is expected that smaller dots and larger Coulomb charging energy are obtained in the valence band than in the conduction band.

Therefore, it is found from the experimental results that smaller dots and higher tunneling barriers are formed in the valence band than in the conduction band. Figure 6 shows a schematic of the possible potential barrier structure.

4. Discussions

Based on the experimental results, the formation mechanism of the dots and the tunneling barriers is discussed. First, the channel width or height fluctuations are considered [1]. In the squeezed point of the channel, the ground state energy in both the conduction band and the valence band is raised due to the quantum confinement effect. As a result, the tunneling barriers for carriers are formed in both bands. If this is the only mechanism, however, the dots would be physically defined dots and the size of the dots formed in both bands should be comparable. This conflicts with the above measurement results. Hence, there must be dots defined as potential wells, not defined physically. At present, the mechanism underlying the formation of the potential wells is not clear, and further study is required.

5. Conclusions

We have investigated the transport properties of the RT operating silicon single-electron transistors and single-hole transistors with an ultra-narrow channel. From the Coulomb blockade characteristics of both electrons and holes in the same physical channel profile, it was found that smaller dots (potential wells) sandwiched between higher tunneling barriers are formed in the valence band than in the conduction band.

References

[1] H. Ishikuro and T. Hiramoto, *Appl. Phys. Lett.* **74**, 1126

(1999). [2] K. Shiraishi, M. Nagase, S. Horiguchi, H. Kageshima, M. Uematsu, Y. Takahashi, and K. Murase, *Physica E* **7**, 337 (2000). [3] S. Horiguchi, M. Nagase, K. Shiraishi, H. Kageshima, Y. Takahashi, and K. Murase, *Jpn. J. Appl. Phys.* **40**, L29 (2001). [4] H. Majima, Y. Saito, and T. Hiramoto, *Tech. Dig. IEDM2001*, p. 733.

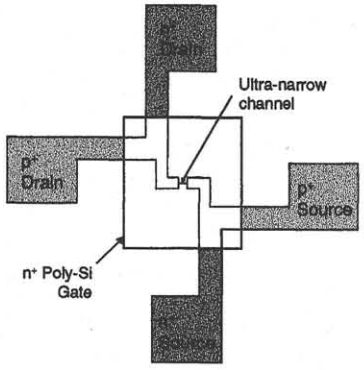

Fig. 1 : Top chematic view of the n- and p-type ultra-narrow channel MOSFET fabricated on an SOI substrate. Both n^+ and p^+ source/drain contacts are formed in a single device. The channel length is 550 nm and the channel width is typically less than 5 nm.

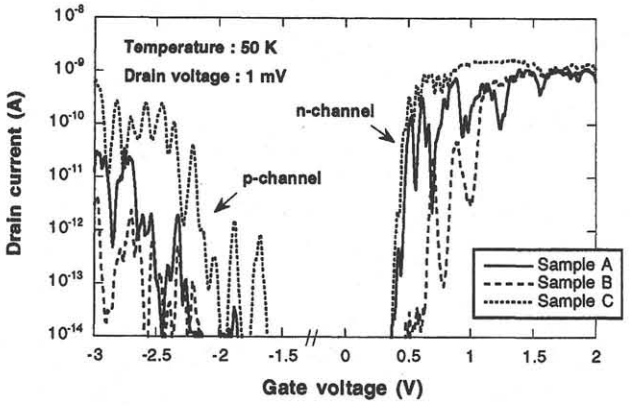

Fig. 3 : Coulomb blockade characteristics in the fabricated ultra-narrow channel MOSFETs at 50 K. In each sample, higher peak-to-valley current ratio is obtained in the p-type region, although some valleys in the p-type region are under the noise level.

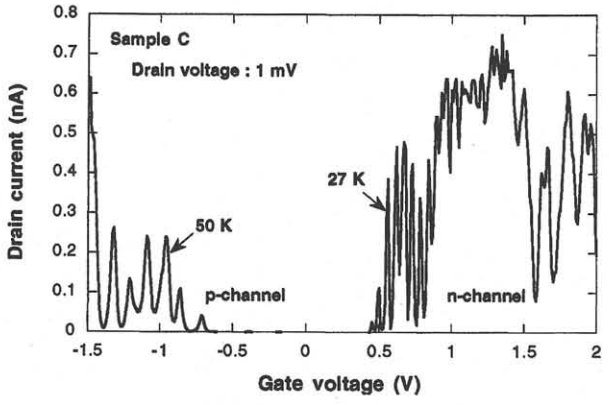

Fig. 5 : Coulomb blockade characteristics in Sample C at 27 K for the n-type region and at 50 K for the p-type region. As in Fig.4, the current peak spacings in both regions are largely different.

Acknowledgements

This work was partly supported by Grant-in-Aid for COE Research (#12CE2004 "Control of Electrons by Quantum Dot Structures and Its Application to Advanced Electronics") from the Ministry of Education, Science, Sports, and Culture, and by the Core Research for Evolutional Science and Technology (CREST) of Japan Science and Technology Corporation (JST).

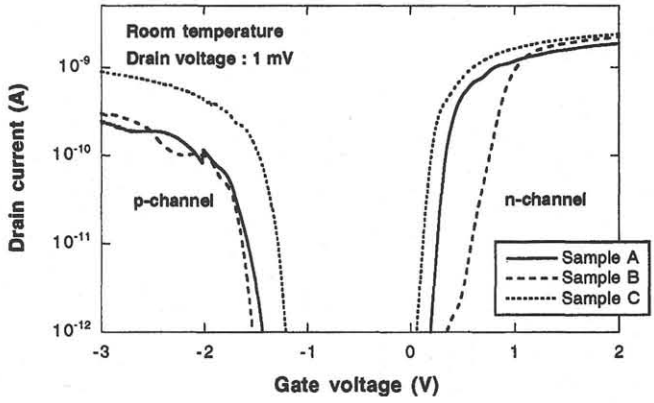

Fig. 2 : Room-temperature Coulomb blockade characteristics in the n- and p-type fabricated ultra-narrow channel MOSFETs. The rapid decrease in the current at $V_g \sim -2$ V in Sample A is probably due to hole injection into the trap in the gate oxide.

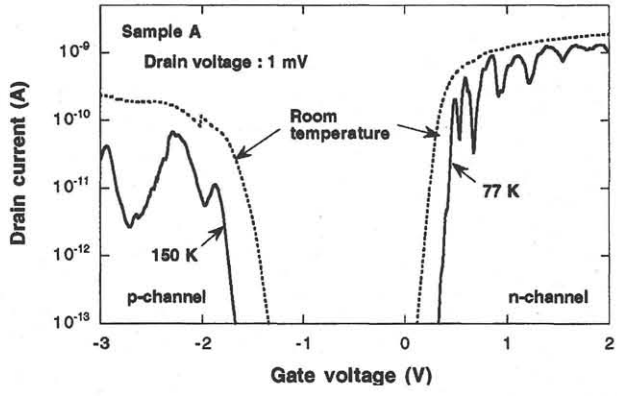

Fig. 4 : Coulomb blockade characteristics in Sample A (ultra-narrow channel MOSFET) at 77 K for the n-type region and at 150 K for the p-type region. The current peak spacing in the p-type region is about three times as large as the n-type region.

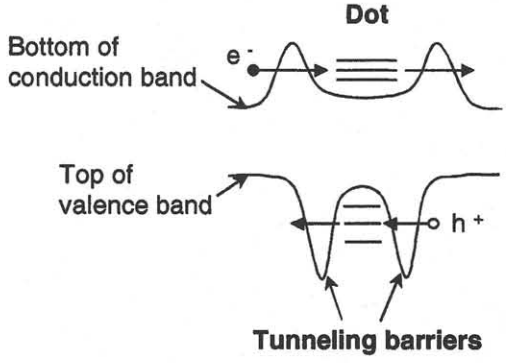

Fig. 6 : Schematic view of the possible potential barrier structure in the fabricated ultra-narrow channel MOSFETs. It is expected that smaller dots (potential wells) and higher tunneling barriers are formed in the valence band than in the conduction band.