Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 110-111

F-2-6

Threshold Voltage of Si Single-Electron Transistor

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1. Introduction

Single-electron transistors (SETs) have been attracting much attention as the ultimate low-power devices. We have already developed a method of fabricating Si SETs with the capacitance of a few aF [1]. The method, called pattern-dependent oxidation (PADOX), can convert a lithographically defined Si wire into a Si island in a self-aligned manner, thereby providing good controllability of island size [2]. Although device-to-device fluctuation in the characteristics between identically designed SETs is still large for LSI application, we expect advances in lithography technology to suppress it, which will enable more precise size-control of the initial Si-wire structure.

On the other hand, offset charges [3] are widely recognized as the most crucial and inevitable issue since they shift the operation point of a SET, which is a highly sensitive electrometer. Because of the randomness of the distribution of the charges, the device characteristics may fluctuate even if device size is completely controlled. Although this argument has often led to a pessimistic view of the practical use of SETs, we think that it is not self-evident and is still an open question as to how strong the offset-charge effect is in actual devices. The most fundamental parameter that should be investigated to clarify that is the threshold voltage (V_{th}) of SETs. However, there have been no experimental reports on V_{th} of semiconductor SETs.

Besides, investigating V_{th} is important from another aspect; it will give us information on the configuration of the conduction-band bottom in Si SETs. The theoretical model of Si SETs by PADOX predicts that the island, which is formed in the central part of the Si quantum wire, is due to the potential well that originates from the band-gap reduction of Si by oxidation-induced strain [4].

In this paper we report for the first time the evaluation of V_{th} of Si SETs. We found that V_{th} was clearly related to a device parameter (the gate capacitance), indicating that there is little fluctuation due to offset charges. The existence of strain in Si was also suggested by the obtained negative V_{th}.

2. Device Structure and Experimental Results

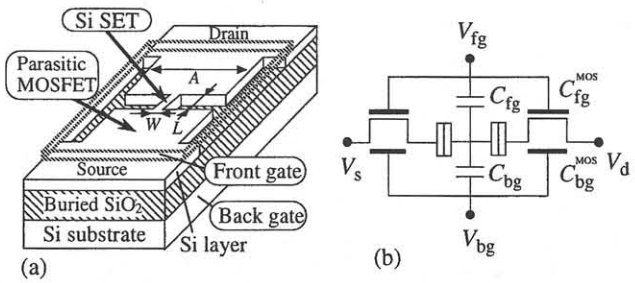

Fig. 1 (a) Schematic top-view and (b) equivalent circuit of the Si SET. The gate oxide is omitted in Fig. 1 (a) for simplicity.

The devices were Si SETs fabricated by PADOX. Figures 1(a) and (b) show a schematic top-view of a SET and its simplified equivalent circuit. A Si wire was formed between the pad Si layers with the width (A) of 400 nm. The initial thickness of the Si wire was 30 nm. The initial width (W) and the length (L) of the Si wire ranged (W=40-50 nm and L=50-100 nm), thereby providing SETs with various island-sizes [2]. After the thermal oxidation, the Si wire was cylindrical with a diameter of the order of 10 nm. Thicknesses of the gate oxide and the buried oxide were 40 and 400 nm, respectively. The potential of the Si island was predominantly controlled by the front gate (n^+ poly-Si) voltage (V_{fg}), and was only slightly modulated by the back gate voltage (V_{bg}). This is because the Si wire was surrounded by the front gate like so-called gate-all-around structures. The ratio of the back gate capacitance (C_{bg}) to the front gate capacitance (C_{fg}) was about 0.01-0.02. As a parameter corresponding to V_{th} for SETs, we evaluated the first-peak voltage (V_{fp}), which was defined as the V_{fg} where the first-electron peak of the Coulomb blockade (CB) oscillation appeared when V_{bg} was fixed at 0 V. It should be noted that V_{fp} could not be directly measured for the present device because the pinch-off characteristics of the parasitic MOSFETs formed on both sides of the SET likely screened the first-electron peak. To avoid this problem, we applied positive V_{bg} to suppress the

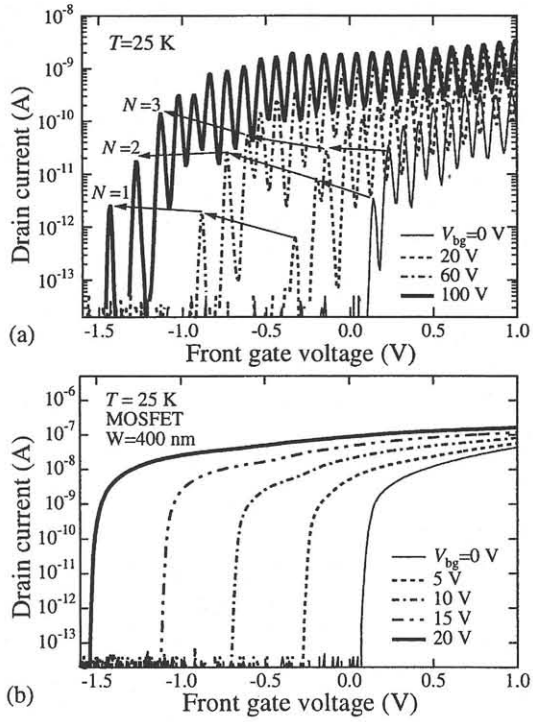

Fig. 2 (a) V_{bg} dependence of I-V_{fg} curves for the SET. The arrows depict the peak shift for the electron number (N)=1, 2, and 3. (b) V_{bg} dependence of I-V_{fg} curves for the 400 nm-wide MOSFET.

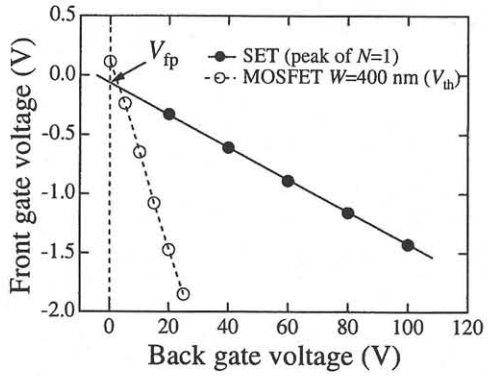

Fig. 3. V_{bg} dependences of the first-electron peak of the SET and V_{th} of the 400-nm-wide MOSFET. V_{fg} is estimated by the extrapolation to V_{bg} = 0 V.

parasitic effect [5]. Figure 2(a) shows V_{bg} dependence of drain-current (I)-V_{fg} curves at 25 K. The source voltage (V_s) and the drain voltage (V_d) were 0 and 3 mV, respectively. As V_{bg} was increased, the first-electron peak appeared. This is because V_{th} of the parasitic MOSFETs was higher than V_{fp} at V_{bg}=0 V, whereas the positive V_{bg} lowered the parasitic V_{th} more than it shifted the first-electron peak of the SET. Figure 2(b) shows I-V_{fg} curves of long-channel MOSFET with the channel width of 400 nm. The ratio between the front and the gate capacitance was 0.085. To describe the situation more clearly, V_{bg} dependence of V_{fg} corresponding to the first-electron peak is shown in Fig. 3, together with V_{bg} dependence of V_{th} of the 400-nm-wide MOSFET. The result clearly suggests that the first-electron peak can be screened by the parasitic MOSFETs at V_{bg}=0 V. Because of the almost linear V_{bg} dependence, however, we could estimate V_{fp} by the extrapolation to V_{bg}=0 V. In this way, we evaluated V_{fp} of various SETs by employing V_{bg} between 0 and 100 V. The results are plotted as a function of the front gate capacitance (C_{fg}) of the SETs in Fig. 4. Here, C_{fg} was estimated from the averaged peak separation for the electron number (N) between 5 and 8, where we could obtain almost periodic CB oscillations. Because a few-electron regime (N <5) likely showed some irregular oscillations, we thought that such an estimation gave a good index of the island size [7]. As shown in Fig. 4, V_{fp} shows a clear relation to C_{fg}; V_{fp} is almost constant and negative for larger C_{fg} and it rapidly increases to positive for smaller C_{fg}.

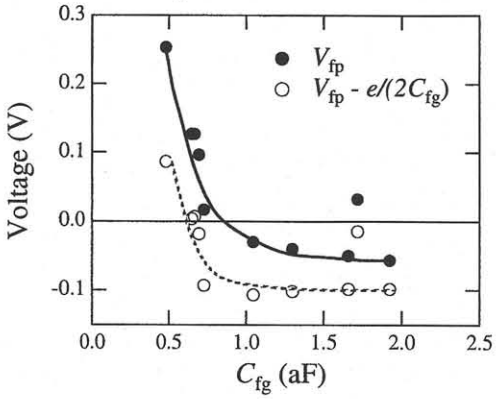

Fig. 4. Relation between V_{fp} and C_{fg} for the fabricated SETs. The plot of V_{fp}- $e/(2C_{fg})$ is also shown. Solid and dotted curves are guides for the eye.

3. Discussion

The clear observation of the relation between V_{fp} and C_{fg} strongly indicates that V_{fp} did not suffer from random offset charges seriously. This is very important from a practical viewpoint because we will be able to control V_{fp} if we can control the size and the shape of the Si island. This might not be surprising when we consider the possibility that interface states and/or oxide charges influence our ultrasmall SETs. The state/charge density of 10^{10} cm^2 corresponds to a single charge per an area of 100 nm x 100 nm, while the Si island size is on the order of 10 nm. In that case, the possibility that the state/charge exists just near the Si island is not strong.

The other important finding is the value of V_{fp} and its dependence on C_{fg}. For larger C_{fg}, V_{fp} was around -0.05 V. If we assume that the classical CB theory is applicable, the conduction-band bottom in the Si island corresponds to V_{fp}-$e/(2C_{fg})$, that is, about to -0.1 V as shown in Fig. 4. On the other hand, the theoretical model of Si SETs [4] predicts that the depth of the potential well at the Si island is about 0.1 eV when 1% strain in Si is assumed. According to the theoretical calculation of V_{th} of a fully-depleted SOI/MOSFET (C_{bg}/C_{fg}<<1) [6], the V_{th} of our Si SETs should almost directly reflect the energy of the conduction-band bottom of Si. Therefore, the obtained values of V_{fp}-$e/(2C_{fg})$~ -0.1 V means that the potential well at the Si island was also 0.1 eV in depth, which agrees well with our theoretical model including oxidation-induced strain. For smaller C_{fg}, V_{fp} showed a rapid increase. The corresponding increase of V_{fp}-$e/(2C_{fg})$ was about 0.2 V. One possible reason for this behavior is the quantum-confinement effect in the Si island. From the theoretical estimation, the quantum-confinement energy reaches around 0.2 eV as the island-size shrinks to 5 nm. A change in the strain might also contribute to the increase of V_{fp}. Gaining a quantitative understanding of these results will be an interesting subject for future work.

4. Summary

Threshold voltages of Si SETs were investigated for the first time. It was found that they showed a clear relation to the gate capacitance, indicating that there was little effect of random offset charges. This is a very important finding that opens up the possibility of V_{th} control towards LSI application. It was also found that the obtained negative V_{th} strongly suggested the bang-gap reduction by oxidation-induced strain in Si.

Acknowledgments

The authors thank Mr. Takayuki Okada at Toyohashi University of Technology for the electrical measurement of the device. The authors also thank Mrs. K. Yamazaki and T. Yamaguchi, and Dr. H. Namatsu for their help in the device fabrication.

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