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The next technology platform based on mobile system and 3D integration

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1. Introduction

Mobile equipment such as a cellular phone currently uses high density multi-layer module technology and 3D stacked package technology to integrate many functions on a several cm square. These technologies have been developed in order to realize high density integration; however it seems to me that they are also effective to realize high performance system. This paper discusses these mobile base technologies as the next technology platform from the view point of high speed signal transfer.

2. Signal transfer model and parameters

The signal transfer can be modeled with driver circuit, receiver circuit, and interconnection circuit as shown in figure 1. Figure 2 shows the cross-sectional view for calculating interconnection parameters. The capacitances for unit length were obtained with taking account of fringe effect and adjacent wires. Table 1 summarizes interconnection parameters.

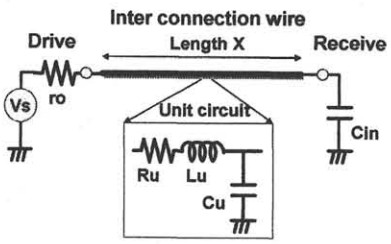

Fig. 1. Signal transfer model.

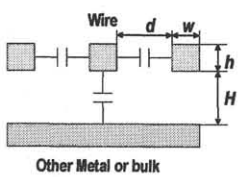

Fig. 2. Cross sectional view.

3. LSI technology and interconnection characteristics

The scaling rule has realized higher frequency operation with lower power consumption, as well as higher integration in LSI technology [1]. However we should pay much attention that the scaling rule contains serious contradiction.

Table 1. Interconnection parameters.

	Local	Global	Supper Connect	Module	PWB
C (fF/mm)	349	254	90	163	113
Rsq(Ohm/mm)	455	227	100	0.01	0.005
RC (ps/mm)	159	57.7	9.02	0.0016	0.00057
L (nH/mm)	—	—	—	1.05	0.47
W (um)	0.22	0.44	1	60	100
h (um)	0.34	0.34	1	60	35
d (um)	0.20	0.40	1	60	100
H (um)	0.79	0.79	3.02	3000	180

The signal propagation delay Tpd can be expressed as following equation approximately [2].

$$Tpd=CuRuX^2+2.2(roCin+RuXCin+roCuX) \quad (1)$$

The propagation delay should be discussed in following three elements.

a) Gate delay

Gate delay: Tpdi is an intrinsic signal delay in MOS transistor shown in the second term of equation (1).

$$Tpdi=K_1L^2/(V_{dd}-V_T) \quad (2)$$

, where K_1 is a proportional coefficient, L is channel length, V_{dd} is operating voltage, and V_T is threshold voltage. If we set S as a scaling factor; L → L/S, V_{dd}-V_T→ V_{dd}-V_T /S then Tpdi→ Tpdi/S. Thus we can reduce the gate delay by scaling rule.

b-1) Local interconnect signal delay

In case of local delay, the RC delay is kept constant with scaling. Because C→C/S due to shortening of interconnection distance and R→SR due to increasing of sheet resistance with factor of S^2 and shortening of interconnection distance with factor of S.

b-2) Global interconnect signal delay

In case of global interconnection, the length increases with increase of chip size. If we set this chip size scale factor as Sc, C→ScC and R→S^2ScR then RC→$(SSc)^2$ [3]. This result shows the signal delay due to the global interconnection will increase rapidly with scaling. The gate delay has been reduced with shrink of design rule; however interconnection signal delay (wire delay) has increased as shown in figure 3 [4]. This suggests that the scaling must not promise the further high speed operation.

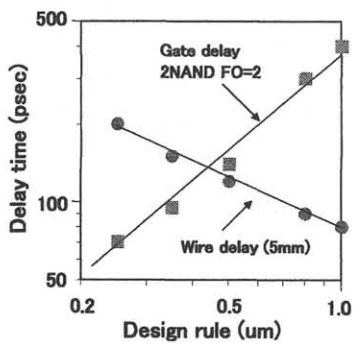

Fig. 3. Gate delay and wire delay trends.

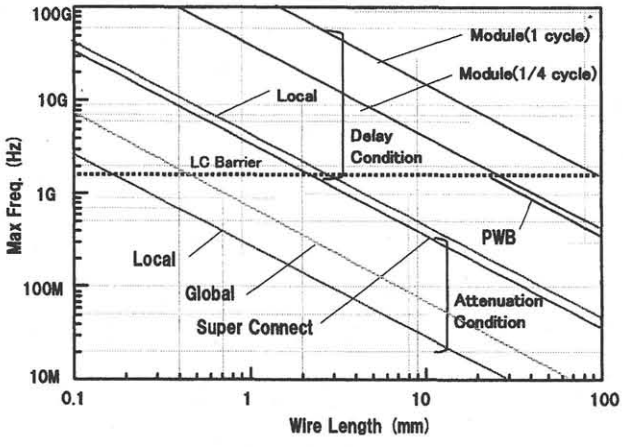

Fig. 4. Maximum operation frequency as a function of wire length in several interconnection methods.

Figure 4 shows the estimations of maximum operating frequency as a function of interconnection length in several methods. The maximum operating frequency has been determined as the frequency at which amplitude decrease of receiving signal is 10% of drive signal or propagation delay is 1/4 or 1 of the data period. Since decrease of amplitude on Interconnection in LSI is large, the maximum operating frequency of LSI is mainly determined by decrease of amplitude. The local interconnection which is longer than 0.2mm can not transfer 1GHz signal. Repeater buffers are often to be inserted to address this issue. Figure 5 shows the maximum operating frequency of LSI when the repeater buffer technique is applied. By using this technology 1GHz signal can de transferred in 1mm long on local interconnection and 4mm long on global interconnection. The super connect technology can increase this distance to 30mm long. However conventional interconnection technology in LSI can not transfer 10GHz signal.

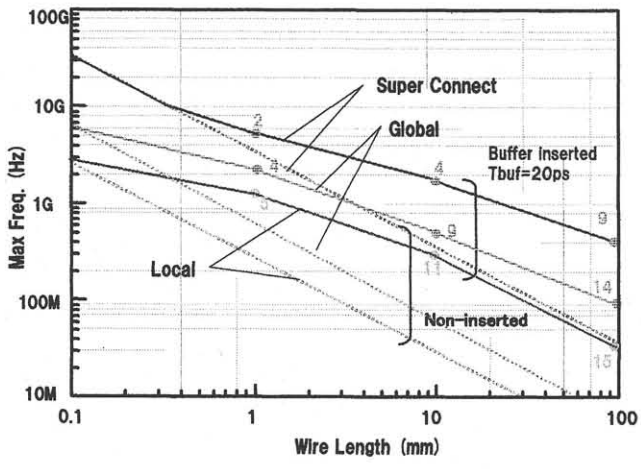

Fig. 5. Maximum operation frequency as a function of wire length when using repeater buffer insertion.

4. PC board and module technology

The signal transfer in PC board or module is not limited by the signal attenuation, but limited by the signal propagation delay. Resistance of wire is low enough for 10GHz signal. Thus 4mm or 15mm signal transfer can be attained for 10GHz signal on module. However we should eliminate the bonding wire and the Large ESD diode to realize high speed signal transfer. Lower resonant frequency due to large inductance of the bonding wire and large capacitance of ESD diode limit the maximum operating frequency at most 1GHz [5]. This limits actual maximum operating frequency of PC board. As a result, the module technology will promise us to realize several GHz operations on 15mm x 15mm square area.

5. Expectation of 3D integration technology

The smaller size is the better for future 10GHz operation system. The size of LSI should be reduced to transfer the high frequency signal. 3D chip integration technology will allow us to use smaller chips, even if the required integration level becomes higher. The total interconnection distance in 3D chip integration system can be reduced to 1/m [6], where m is the chip reduction ratio. Thus 10GHz operation will be realized easily by using 3D chip integration technology with small chips whose size is smaller than 7.5mm x 7.5mm.

6. Conclusion

Interconnect signal delay and amplitude decrease at high frequency signal in LSI seems serious. Several GHz operations look very tough essentially. In contrast, the mobile base module technology and 3D integration technology must have a high potential to be the next technology platform to realize the several GHz systems, as well as to realize low power operation.

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