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High Performance, Low Power Three-Dimensional Integrated Circuits for Next Generation Technologies

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1. Introduction

Three-dimensional (3-D) circuit integration is an enabling technology that allows independently fabricated circuit layers to be stacked and electrically interconnected in the vertical dimension. 3-D integrated circuits have the potential for very high bandwidth data paths between processor and memory blocks. They will allow substantial savings in systems power arising from reduced line capacitance and a lessened need for inter-chip communications.

These at least are the claims of 3-D circuit technology proponents. A hesitant multi-billion dollar semiconductor industry is listening, but is not yet thoroughly convinced. It is aware of one fact—that significant improvements in circuit performance and on-chip system integration are becoming exponentially more expensive to achieve.

This paper describes past and on-going work in the development of 3-D circuit architectures, which we believe can illustrate both the need for and the benefits of 3-D integrated circuit technology. Six years of research into these designs have convinced us that the benefits of 3-D integration will come, not just from relieving current I/O bottlenecks, but in opening the door to a new generation of applications that cannot be realized in 2-D technology. The two applications we will discuss here are smart focal plane arrays and processor-in-memory embedded systems.

2. 3-D Smart Focal Plane Architectures

Image sensing and processing are applications that clearly require high I/O bandwidth. Conventional 2-D solid-state imagers, whether CCD or CMOS, incur an exponential cost penalty when scaled to large array sizes. This is because picture quality and resolution requirements impose tight pixel pitches (~10μm) and high fill factors. If there is any on-chip processing, it happens at the edges of the array, where at most one row or column can be processed at a time. A 3-D smart focal-plane architecture, however, can simultaneously permit small pixel sizes, 100% fill factor, pixel-parallel processing, and fully digital pixel data storage and readout.

With the support of the Defense Advanced Research Projects Agency (DARPA) of the U.S. Department of Defense, we have designed and fabricated increasingly complex 3-D smart focal plane architectures over the last several years. One of the first designs, originally presented at the IEEE International Solid State Circuits Conference in 2001, was a 2-layer device containing an A/D converter per pixel [1]. This circuit was fabricated at MIT Lincoln Laboratory using a partially depleted 0.8μm SOI/CMOS process for the circuit and photodiode wafers.

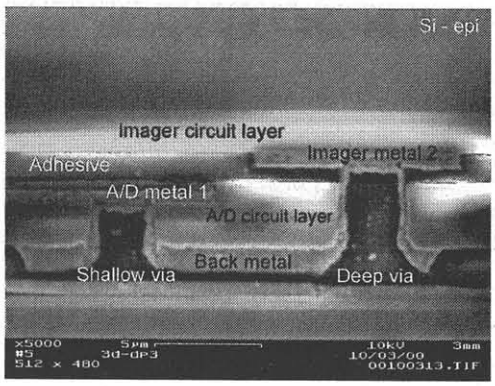

Figure 1. SEM of 3-D deep and shallow via pair in first 2-layer imager.

The use of SOI wafers is one method to facilitate 3-D assembly since the circuits are contained in thin silicon films, which can be transferred to a multi-layer stack. The buried oxide (BOX) functions not only as an excellent etch stop when removing the handle wafer from the circuit layers, but also as an insulator for metal vias that form vertical interconnects between the layers. In the process used to assemble the first 3-D imager, the vertical interconnect was formed by defining a "shallow" and "deep" via pair as shown in the scanning electron micrograph of Fig. 1.

A 64 x 64 test imager was implemented in this manner. The pixel-parallel circuit design, described in [2], permitted response to a very wide range (over 100dB) of incident light intensities. Power consumption per pixel was approximately 60nW/pixel at VDD=3V under average room lighting conditions. A sample raw image taken by the 3-D sensor is shown in Figure 2.

Following this first prototype, the 3-D focal plane architecture was expanded to include three layers: one for

the photodiode array, and two for pixel processor circuits containing arithmetic-logic functions and refreshable DRAM storage. MIT Lincoln Laboratory is currently fabricating this design, whose floorplan is shown in Fig. 3., in a fully-depleted 0.18μm SOI process. The unit pixel laid out for this process measures 14.5μm x 14.5μm.

Figure 2. Picture taken by first 2-layer 64x64 3-D imager

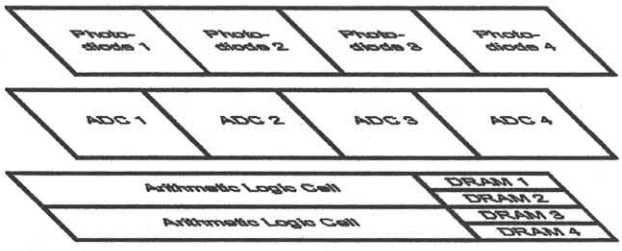

Figure 3. Floorplan for new 3-layer high-resolution imager

This 3-layer focal plane architecture will permit photographic-quality imaging for both still frame and video capture. Pixel-parallel processing means that the imager can be scaled to arbitrarily large sizes without timing becoming a limiting factor. There is no need to transfer analog data across long bus lines and to digitize it at high speeds.

3. 3-D Processor-in-Memory Architectures

A significant driving force for 3-D integration is the increasingly difficult problem of communicating data between the CPU and memory in modern digital microprocessors. Computational RAM, or C-RAM [3], is a processor-in-memory architecture that takes advantage of the large internal memory bandwidth available at the sense amplifiers. A team at the University of Alberta has developed a fully modular 3-D C-RAM architecture in which a single mask set can be reused for multiple layers. Dies can be separately addressed and achieve the necessary inter-processor communication, regardless of the number of layers in the 3-D stack. The design embodies a novel fault tolerance scheme for maintaining data processing consistency in the presence of defective memory columns and partially defective processing elements.

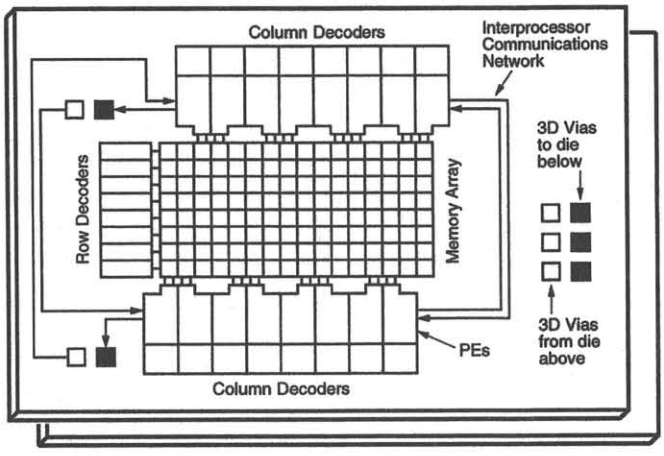

Figure 4. 3-D C-RAM Architecture

The new 3-D C-RAM architecture is diagrammed in Fig. 4. A test chip, with 128 kb of memory and 512 processing elements is being fabricated in the MIT 3-D process along with the 3-layer imager. Simulations predict that the chip will achieve 170 billion bit-operations per second at 400 MHz.

4. Conclusions

Two novel architectures have been presented for next generation 3-D systems. We hope these examples will motivate further development of both new 3-D circuits and assembly process technologies.

Acknowledgments

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References

[1] J. A. Burns et al, "Three-dimensional integrated circuits for low-power, high-bandwidth systems on a chip", in Proc. IEEE Int. Solid-State Circuits Conf., pp. 268–269, 453, February 2001.

[2] L. McIlrath, "A low-power low-noise ultrawide dynamic-range CMOS imager with pixel-parallel A/D conversion." IEEE J. of Solid-State Circuits, vol. 36, n. 5, pp. 846–853, May 2001.

[3] J. C. Koob, et al, "Design of a 3D Fully-Depleted SOI Computational RAM", Proc. Euro. Solid-State Circuits Conf., Paper C-149, September 2002.