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Genuine Technologies for Three-Dimentional (3D) LSI

Katsuya Okumura and Nobuo Hayasaka*

Research Center for Advanced Science and Technology, The University of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo 153-8904, Japan
Phone:+81-3-5452-5324 Fax:+81-3-5452-5184 E-mail: okumura@su.rcast.u-tokyo.ac.jp
* Semiconductor Company, Toshiba Corp.
8 Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan

1. Introduction

In the past 30 years, the main driver of semiconductor industry has been the computers. The focus now is shifting to the consumer electronics. The main device for computers is commodity DRAM, which is expected to produce ten millions of chips monthly over several years. On the other hand, the consumer electric customers require original LSIs, yet the orders for custom LSIs are three or four digits smaller than those for DRAMs. And the lifecycle of the device is only 6 months or less. The total product number is less than one ten thousandth of commodity DRAM. These same customers also are demanding quick turnaround time (QTAT) to reduce the risks from consumer products.

To provide the high-performance custom LSI, SOC (System on a chip) device has been proposed. So far as high cost and massive product volume is allowed, this SOC is the best solution. The real world, however, requires the low-cost chip, QTAT and small volume. This is a paradigm shift of semiconductor industry. We have to change drastically the both fields of the device design methodology and the device manufacturing. One answer to solve this challenge is an agile manufacturing method based on a mini-fab concept rather than the current mega-fab concept.

Another innovative approach is 3D LSI. In the past, only a two-dimentional space has been used, but the focus is now shifting to the possibility and the merits of three-dimentional array. Fig. 1 shows the final structure of the 3D device. The thickness of each chip and each interposer is in a range of 30μm, where the inter-chip connection is made by using a Cu direct bonding technology. The merits of the 3D LSI are as follows.

Any chip with different design rules and different nature such as MOS, Bipolar and compound LSI can be integrated into a single 3D LSI. This architecture enables the system designers to reuse the devices already developed in the past, which leads to the low development cost and the QTAT.

2. Fabrication Process of 3D LSI Chip

Via holes that go through the entire chip are formed using RIE technology on the wafer which is finished the FEOL process. The size of via-hole is 20μm in diameter and 30μm in depth. A SiN diffusion barrier layer is deposited, followed by Cu-fill using electro plating and Cu-CMP, as shown in Fig. 2-(1). This process will leave Cu only in the via holes. Then the metal interconnect layers are constructed as M1, M2 and so on until it completes the BEOL process (Fig.2-(2)).

A wafer-level burn-in test is carried out so as to extract the good dies on this whole wafer. After this process, the wafer is etched off 600μm or more to the level of the Cu vias (Fig.2-(3)). At this point, the thickness of the wafer is in the range of 30μm. All KGDs (known good die) are chosen. Each thin KGD is laminated and is connected using Cu direct bonding technology. By repeating this step, the 3D LSI shown in Fig.1 will be completed. In order to realize this 3D LSI device, the following technical challenges are waiting ahead of us.

3. Technical Challenges

High-rate RIE & High-rate Plating

There is no technical difficulty as to via patterning and via metal filling. The problem lies in the productivity and process costs. The conventional RIE and electroplating are done at a rate of 1μm per minute, which will result in extremely low throughput. In order to overcome these problems, high-rate RIE and high-rate plating will be necessary. I, Sakai et al.[1] already demonstrated the feasibility of a high speed RIE at a rate of 30-50μm per minute. Regarding the high speed plating, the highest rate we can obtain today is approximately 5μm per minute by using a immersion plating technology.[2] Further acceleration of plating speed and, if possible, high-rate electro-less plating technology is highly needed.

Cu-Cu Direct Bonding

The number of the connections between Cu pads and Cu vias will reach several ten thousands. The conventional soldering will not provide sufficient production yields and reliability. The Cu-Cu direct bonding technology should be developed to solve the problem. Ultraplanar Cu CMP and a removal of Cu oxides from Cu surface are important to achieve the technology. The ultraplanar clean metal surface will be probably bonded without any solder when some pressure and temperature is supplied. The point of this technology is to lower the pressure and the temperature while keeping the low process cost and the high yield. Cu oxide is more easily removed than Al oxide. Consequently, Cu interconnect system has an advantage over Al system in terms of the direct bonding technology. One remaining issue is how to hold on the clean Cu surface after CMP.

KGD Probing

In order to secure the reasonable yield on the 3D LSI, only KGDs should be used for final assembly. The probing test should be carried out at high frequency after high temperature burn-in test. Cu interconnect system has some advantages and disadvantages compared to Al system. One of the advantages is the softness of Cu oxides comparing to Al oxides, which makes the probing much easier. On the other hand, Cu is more sensitive to oxidation and it can not be exposed to high temperature in air. Therefore, the burn-in test has to be done in an oxygen-free environment. It will be impossible to use conventional tungsten wire probe for the probing test because of floating capacity, inductance and a pad layout. The probes with a minimum length and a vertical alignment must be used. Moreover, the contact force per probe will become a more important issue since the number of pads will reach several thousands.

Ultra-low contact force probing technology has been developed, which is using a kind of electric breakdown known as fritting. We demonstrate[3] that the probing is possible even at a lower contact force than 0.1g per pad by applying the fritting to Cu pad.

4. Summary

The concept of 3D LSI is proposed to solve several critical issues which semiconductor industry will face in the near future, and most of those critical issues are believed to be solved by adopting this concept. We will have to keep on challenging to create new technologies which lead 3D LSI. The biggest challenge is to increase the productivity of relatively large and thick patterning, while keeping the costs low. Some of the technologies proposed in this paper will become key technologies in this century and they will probably affect other industries such as MEMS and biotechnologies.

References

(1) I. Sakai et al.; Proc. of the 1st International Symp. on Dry Process, 57 (2001).
(2) M. Tsujimura et al.; Proc. of ISSM, IEEE (2000).
(3) K. Kataoka et al.; to be presented at International Test Conf. 2002.

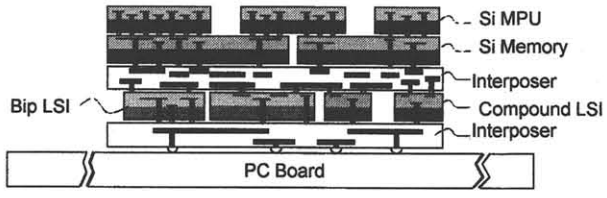

Fig.1 Crosssection figure of 3D LSI

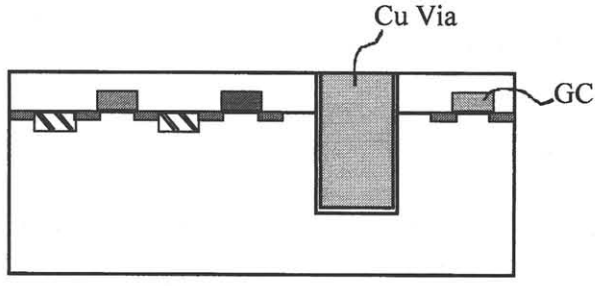

Fig.2-(1) Deep Cu via (20φμm x 30φμm)

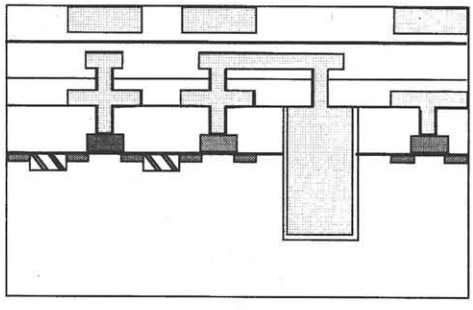

Fig.2-(2) BEOL process

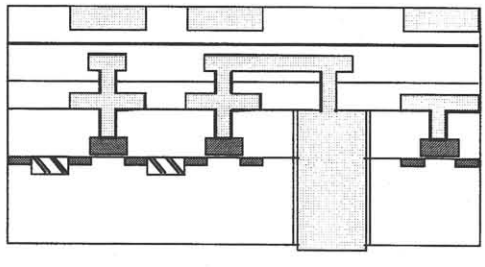

Fig.2-(3) Wafer thinning

Fig.2 Fabrication process of 3D LSI chip