Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 316-317

F-4-4

Thermal Analysis of Self-Heating Effect in Three Dimensional LSI

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1. Introduction

Three-Dimensional (3D) integration is the most promising technology to improve the LSI performance by reducing the wiring delay and increasing the interconnection density. However, 3D LSI has a concern of increasing heat accumulation as a result of vertically stacking many chips and isolating them with insulating materials with low thermal conductivity. Several works about the heat generation and accumulation in 3D LSI have been reported so far[1,2]. However, these works describe mainly the results obtained by the computer simulation.

In this work, we evaluate the heat generation and accumulation in 3D LSI by directly measuring the chip temperature using fabricated 3D LSI test chips. Furthermore, we compare the experimental results with those obtained by the simulation to reveal the mechanism of thermal flow in 3D LSI.

2. Simulation Results

First of all, we carried out the thermal analysis for 3D LSI using ANSYS simulator. Figure1 shows the structure of 3D LSI test chip for thermal analysis. Three device layers were stacked vertically and glued to the backside of quartz glass wafer. These layers are electrically connected each other by the vertical interconnections which consist of the buried interconnections and the metal microbumps. The structure used in the simulation consists of silicon, silicon dioxide, aluminium wiring and indium microbump. Insulating materials are inserted between device layers. The bottom of chip was fixed at the room temperature to give a boundary condition. A heat source to represent a heat generated by the power consumed in 3D LSI chip is placed at the surface of the top device layer underneath the quartz glass. The total power consumption is assumed to be $23W/cm^2$. The simulated temperature profile and heat flow are shown in Fig.2 It clearly demonstrates that the generated heat flows mainly through the vertical interconnections. Especially, it is clearly shown that the metal microbumps surrounded by the insulating materials give rise to effective thermal paths between Si substrates. Figs.3 (a) and (b) show the maximum chip temperature dependence on the sizes of microbumps and buried interconnections, respectively. The maximum chip temperature is represented as the temperature relative to one at the bottom of the chip. As is clear in the figure, the maximum chip temperature decreases with increasing the cross-sectional size of vertical interconnection because the vertical interconnections more effectively act as the heat sinks.

3. Experimental Results

In order to confirm the validity of simulation results, we directly measured the temperature rises in fabricated 3D LSI test chips. The SEM cross-sectional view of 3D LSI test chip is shown in Fig.4. It consists of three device layers and one thick quartz glass layer which acts as the supporting material. The SEM cross section clearly shows that these layers are tightly glued and connected by the buried interconnections and metal microbumps. The thickness of each silicon substrate is around 30 μm and the thickness of the insulating layer between device layers is around 4 μm. Figure 5 briefly describes the structure of test chip to evaluate the self-heating effect in 3D LSI chip. Poly-Si heater which can generate the heat corresponding to the power consumption of $28W/cm^2$ was formed in the first layer just under the quartz glass wafer. The p-n diodes were formed in each layer to measure the temperature. Several modules with various kinds of test patterns are installed in a 3D LSI test chip. The vertical interconnections with the cross-sectional size of 12×2 μm were placed surrounding the heater and the diodes in some test modules. Test modules had different area ratios of 0, 3, 5 and 7%. Te area ratio is defined as the ratio of the total cross-sectional area for vertical interconnections to the module area. The currents for the heater and the p-n diodes were supplied through the vertical interconnections. First of all, the capability of p-n diode as a temperature sensor was evaluated by measuring the temperature dependence of I-V characteristics of p-n diode. Figure 6 shows the dependence of p-n diode forward voltage drop at the forward current of $0.1\ \mu A/\mu m^2$ on the chip temperature. Excellent linearity between the voltage and temperature was obtained and hence p-n can be used as an excellent temperature sensor. Using such p-n diode, we measured the temperature rise of a chip for various cross-sectional areas of vertical interconnections as shown in Fig.7. The power of $23W/cm^2$ was supplied for the heater. It is obvious from the figure that the maximum temperature decreases and in addition the temperature in three layers approaches the identical value as the cross-sectional size of vertical interconnections is increased. Figure.8 shows the temperature differences between the first layer and the third layer as a function of the cross-sectional sizes of vertical interconnections comparing the experimental results with the simulation results. As is clear in the figure, excellent agreement was obtained between them.

4. Conclusions

We fabricated 3D LSI test chip and directly measured

the chip temperature to confirm the validity of the simulation results. Excellent agreement was obtained between the experimental results and the simulation results. We also revealed that the vertical interconnections effectively work as good heat sinks in 3D LSI.

Acknowledgments

This work was performed in Venture Business Lab., Tohoku Univ, and partly supported by CREST (Core Research for Evolutional Science and Technology) of Japan Science and Technology Corporation (JST) and Association of Super-Advanced Electronics Technologies (ASET).

References

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[2] T. Y. Chiang, S. J. Souri, C. O. Chui and K. C. Saraswat, *Tec. Dig. Int. Electron Device Meeting 2001* (2001) p.681

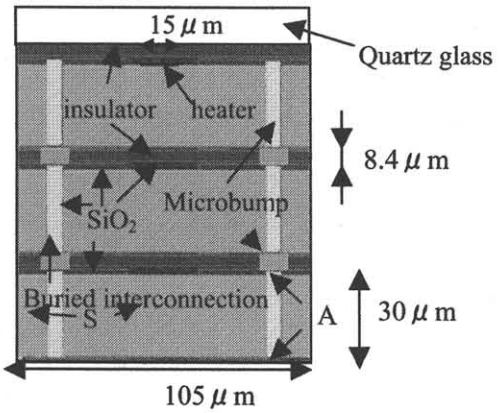

Fig. 1 Cross-sectional view of 3D test structure used in the simulation.

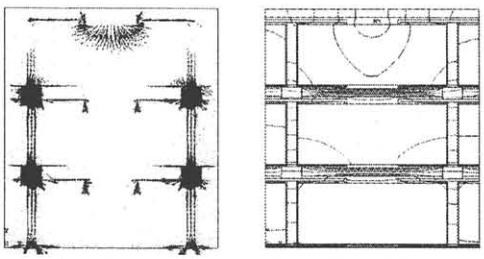

Fig.2 Temperature profile and heat flow.

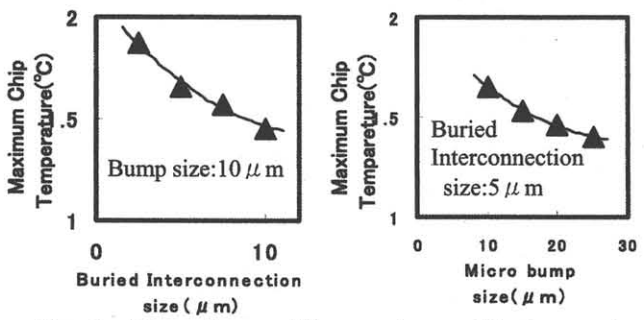

Fig. 3 Dependence of the maximum chip temperature on the cross-sectional sizes of vertical interconnections.

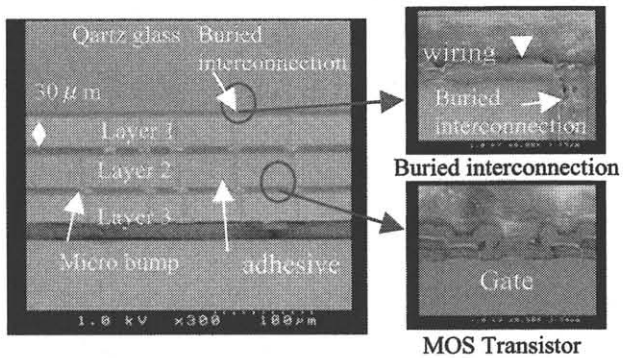

Fig.4 SEM cross sectional view of 3D LSI test chip.

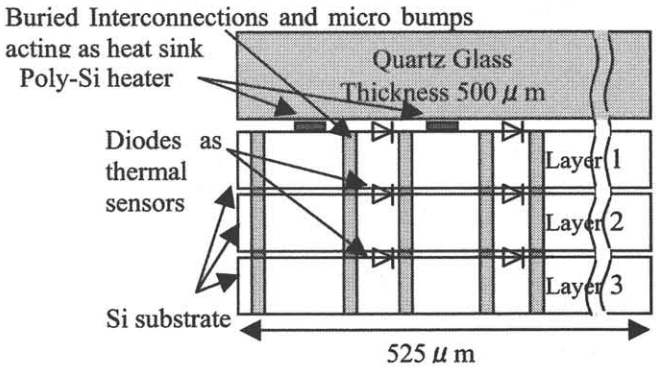

Fig. 5 Cross-sectional view of fabricated 3D test structure used in the experiment.

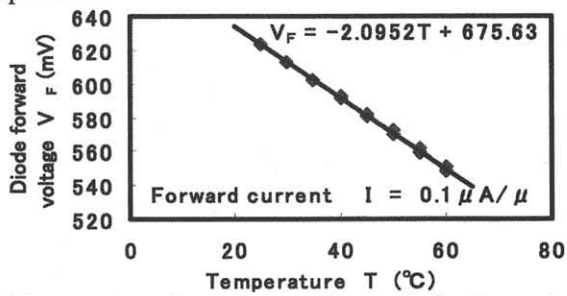

Fig. 6 Temperature dependence of p-n diode forward voltage drop.

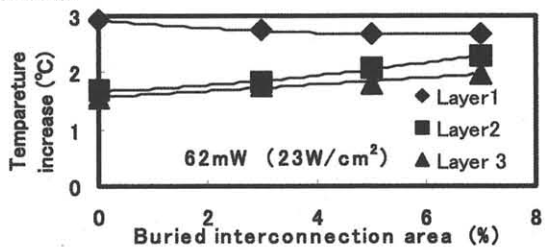

Fig.7 Temperature increase as a function of cross-sectional area of buried interconnection.

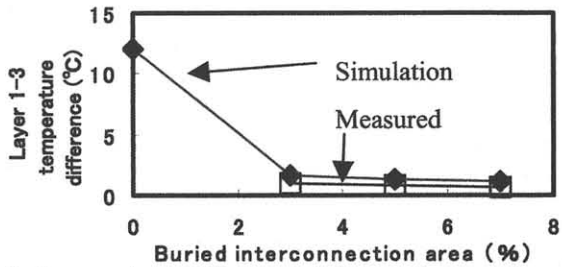

Fig.8 Temperature differences between the first layer and the third layer as a function of the cross-sectional sizes of vertical interconnections comparing the experimental results with the simulation results.