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Novel Nonvolatile Random Access Memory with Si Nanocrystals for Ultra Low Power Scheme.

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1. Introduction

Devices with nanocrystals in the floating gate [1-3] are candidates for substitutes for flash memories because of their capability in low voltage operation. However, there has been no report on memory cell array or write/erase operation suited to such quantum effect memories. We have developed a random access memory for ultra low power operation. It consists of novel quasi-nonvolatile memory device having Si nanocrystals. The memory cell has the following characteristics: random accessible; non-destructive readout; low operation voltage; small cell size of $4F^2$(F: feature size). These characteristics are realized by the well-bitline technology and the novel memory device with a functional floating gate which is composed of a thin poly Si film and Si nanocrystals.

2. Device Fabrication

Fig.1 is the schematic cross-section of the memory device. The memory device has a MOSFET with a floating gate composed of a thin poly Si film and Si nanocrystals. The thin poly Si film and Si nanocrystals are separated by SiO_2 or SiN film. Only oxidation (or SiN deposition) and Si deposition process (LPCVD) were repeated to form the floating gate. Poly Si film (~5nm) was formed through first LPCVD and Si dots (~5nm) were nucleated through the following (2nd and 3rd) LPCVD. Formation of the poly Si film and the Si dots had been achieved using the same condition of LPCVD. Growth of the poly-Si film or that of the Si dot was spontaneously determined by the foundation layer. Thin poly Si film grew on oxidation film of single crystal Si, and dots grew on that of poly crystal Si or on LPCVD SiN. Si nanocrystals are classified into two; located close to the Poly Si film and slightly above (see Fig.2), which correspond to ones formed during 2nd LPCVD and 3rd LPCVD, respectively.

3. Results and Discussion

Figs.3 and 4 show the schematic view of the memory cell array. Source and drain regions are connected to bitline1 and bitline2, respectively. Moreover shallow p-well is divided by trench isolations into plural wiredrawn regions, which act as bitline3 (well-bitline). The cell area was reduced to $4F^2$ using winding trench isolations, which separate the source/drain from the neighboring one in the direction of a word line. The well-bitline has an important role in random access operation. Using the well-bitline, the potential of shallow p-well can be changed independently without interference between the neighboring cells connected to the common word line.

Fig.5 is the circuit of the memory cell array and Tables I and II show the electric field at selected and unselected cells on writing and erasing operation, respectively. In writing mode, 3V is applied to selected word line and 0V to selected bit lines, so the potential of the control gate (Vg) is 3V against source, drain and well at the selected cell. On the other hand, only 1V or -1V is biased at unselected cells. In erasing mode word line is –3V against bit lines at the selected cell, while 1V or -1V at unselected cells. The novel memory device has suitable characteristics for this operation as shown in Fig.6. Hysteresis was appeared when word voltage was swept to +3V or -3V. However, no hysteresis was observed at the ranges between -1V and +1V. These results can make a significant contribution to realize the writing or erasing operations only on the selected cell when these operations are performed with voltages as shown in tables I and II. It means random access is possible. In reading mode voltages applied to control gate and drain are within 1V. Therefore, data are not destroyed during the readout operation in this memory device. Figs.7 and 8 show the writing/erasing and retention characteristics, respectively. It was confirmed that the memory operation at low voltage was realizable.

Remarkably large quantum effect was observed in another device fabricated under different condition. Fig.9 shows the notable example of Id-Vg characteristic of the sample, which had thinner poly Si film than that shown in Fig.6. The drain current reduced abruptly at about 1V. The significant reduction by the order of 10^4 was achieved. It implies that electrons were injected into the floating gate in unison at 1V by tunneling.

4. Conclusions

We have investigated a novel memory device having Si nanocrystals, which can be written or erased at +3V or -3V and read at 1V. This memory device is applicable to the memory cell having features of random accessible, non-destructive readout, low voltage operation and small size of $4F^2$.

References

[1] S.Tiwari, et al., IEDM Tech. Dig. 1995, pp.521-524.
[2] Y.King, et al., IEDM Tech. Dig. 1998, pp.115-118.
[3] R.Ohba, et al., Ext. Abs. of 2001 Int. Conf. on SSDM, p.590.

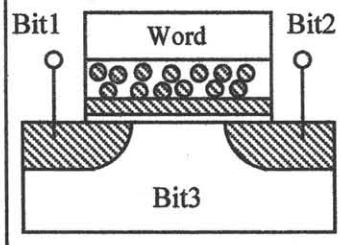

Fig.1 Schematic cross section of memory cell.

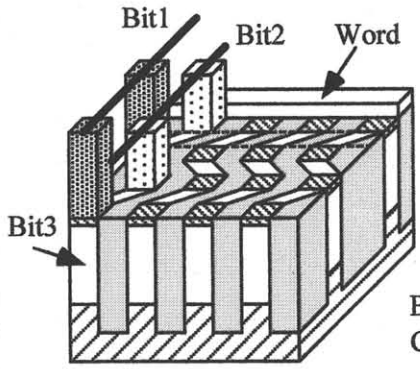

Fig.3 Schematic bird's view of random access dot memory.

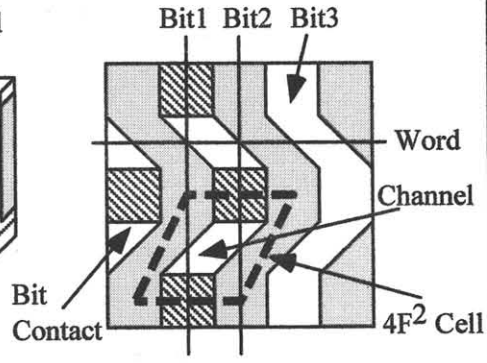

Fig.4 Schematic plan of memory cell array.

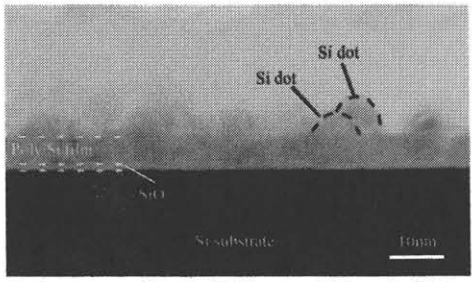

Fig.2 Cross-sectional TEM image of thin poly Si film and Si nanocrystal dots. Control gate is not formed.

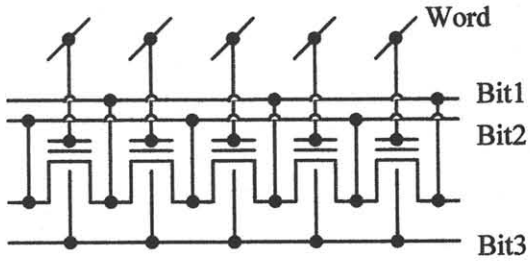

Fig.5 Circuit of memory cell array.

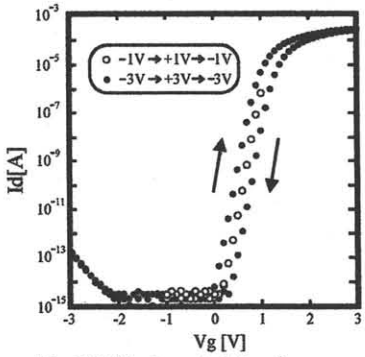

Fig.6 Id-Vg characteristic of memory device.

Table I Electric field in writing mode.

Writing Mode		Selected Word 3V	Unselected Word 1V
Selected	Bit1 0V	Select 3V	Unselect 1V
	Bit2 0V		
	Bit3 0V		
Unselected	Bit1 2V	Unselect 1V	Unselect -1V
	Bit2 2V		
	Bit3 2V		

Table II Electric field in erase mode.

Erase Mode		Selected Word 0V	Unselected Word 2V
Selected	Bit1 3V	Select -3V	Unselect -1V
	Bit2 3V		
	Bit3 3V		
Unselected	Bit1 1V	Unselect -1V	Unselect 1V
	Bit2 1V		
	Bit3 1V		

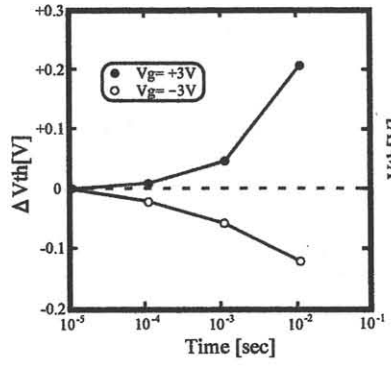

Fig.7 Write/Erase characteristics.

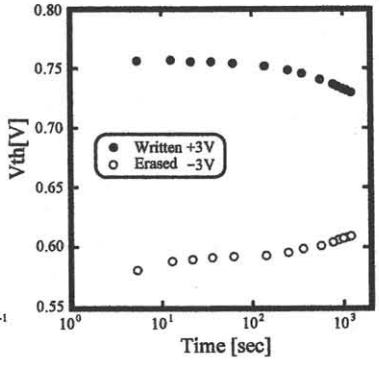

Fig.8 Retention characteristic.

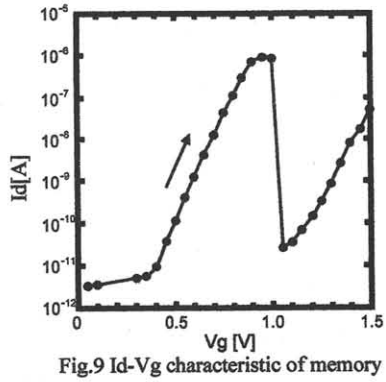

Fig.9 Id-Vg characteristic of memory device (poly Si film is thinner than that shown in Fig.6).