Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 116-117

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InP-Based HEMTs with a Very Short Gate-Channel Distance

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1. Introduction

InP-based $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ high electron mobility transistors (HEMTs) are the most promising devices for sub-millimeter-wave (300-GHz to 3-THz) applications. In our previous works [1-6], we fabricated decananometer-gate lattice-matched (x=0.53) and pseudomorphic (x=0.7) HEMTs. The minimum gate length L_g is 25 nm [3,4], and the record cutoff frequency f_T is 472 GHz [6]. Moreover, we confirmed that increasing the In content in the InGaAs channel layer [5] and reducing the gate-channel distance [6] can effectively increase f_T, and we pointed out that the channel aspect ratio defined as $\alpha = L_g / (d + d_c)$, where d is the gate-channel distance and d_c is the channel layer thickness, must be increased to more than 1 to suppress a marked short-channel effect for sub-50-nm-gate HEMTs [4]. In this work, we fabricated decananometer-gate InAlAs/InGaAs HEMTs by using the concepts and techniques developed in our previous works [1-6]. We reduced the gate-channel distance to keep the channel aspect ratio greater than 1.

2. Device Fabrication

Lattice-matched and pseudomorphic HEMT epitaxial layers were grown on semi-insulating (100) InP substrates by metalorganic chemical vapor deposition. In the lattice-matched HEMTs, the layers, from bottom to top, consist of a 300-nm InAlAs buffer, a 15-nm InGaAs channel, a 3-nm InAlAs spacer, a Si-δ-doped sheet (5×10^{12} cm^{-2}), a 10-nm InAlAs barrier, a 6-nm InP, and a 30-nm Si-doped InGaAs cap (1×10^{19} cm^{-3}) layer. In the pseudomorphic HEMTs, the $In_{0.7}Ga_{0.3}As$ channel layer is 12 nm thick, the $In_{0.53}Ga_{0.47}As$ cap layer is 40 nm thick, and the other layers are the same as those in the lattice-matched HEMTs.

The fabrication process was similar to that used in our previous works [3,4]. Source and drain ohmic contacts with a spacing L_{sd} of 2 μm were formed by using non-alloyed Ti/Pt/Au. T-shaped Ti/Pt/Au Schottky gates with widths W_g of 50 x 2 μm were fabricated by using electron beam lithography and a standard lift-off technique. A two-step-recessed gate [7] was used to reduce the gate-channel distance to 4 nm, while keeping a higher electron-sheet density in the side-etched region of the gate recess.

3. Results and Discussion

S-parameters were measured at frequencies up to 50 GHz in 0.25-GHz steps. Note that the parasitic capacitance due to the probing pads was carefully measured and subtracted from the measured S-parameters by using the same method as in our previous work [3]. Figure 1 shows the frequency dependence of the current gain $|h_{21}|^2$ of a 25-nm-gate lattice-matched HEMT under a drain-source voltage V_{ds} of 0.8 V and a gate-source voltage V_{gs} of 0.35 V. We obtained an f_T of 500 GHz by the extrapolation of $|h_{21}|^2$ using a least-squares fit. This f_T is superior to the value obtained for our HEMT that has a thicker barrier layer [3,4]. Figure 2 shows the frequency dependence of the current gain $|h_{21}|^2$ of a 25-nm-gate pseudomorphic HEMT under a V_{ds} of 0.8 V and a V_{gs} of

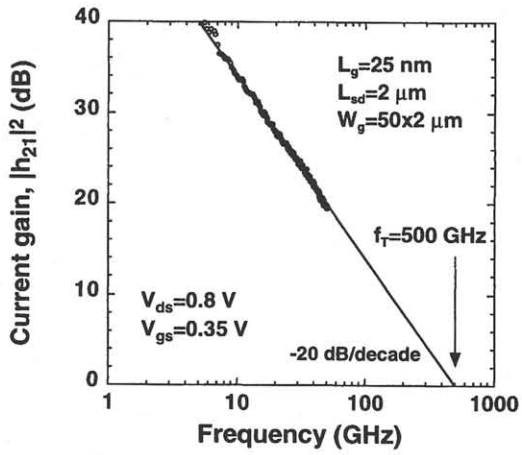

Fig. 1 Frequency dependence of the current gain $|h_{21}|^2$ for a 25-nm-gate lattice-matched HEMT.

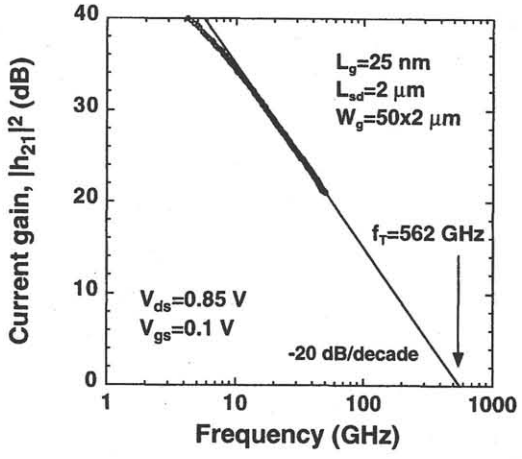

Fig. 2 Frequency dependence of the current gain $|h_{21}|^2$ for a 25-nm-gate pseudomorphic HEMT.

0.35 V. We obtained an ultrahigh f_T of 562 GHz, which is the highest value ever reported for any transistor.

Figure 3 shows the L_g dependence of f_T in our present and previous works [1-6]. The values adjacent to the symbols indicate the channel aspect ratios determined by using cross-sectional transmission electron microscope images. The dotted line is the calculated one using the equation

$$f_T = [2\pi (\tau_{ex} + L_g / v_s)]^{-1}, \quad (1)$$

where τ_{ex} is the extrinsic delay time (= 0.25 ps), and v_s is the saturation velocity (= 2.6 x 10^7 cm/s). The values of f_T in our earlier works for lattice-matched HEMTs [1-4] are close to the values shown by the dotted line. By increasing the channel aspect ratio from 0.83 to 1.3, the f_T was increased from 396 to 500 GHz for the 25-nm-gate HEMTs. As can be clearly seen from Fig. 3, a larger channel aspect ratio, i.e., a shorter gate-channel distance at the same gate length, generally provides a higher f_T. The dashed lines are the "iso-ratio" lines with $\alpha = \sim 1.1$ and 1.6. Thus, reducing the gate-channel distance increases f_T.

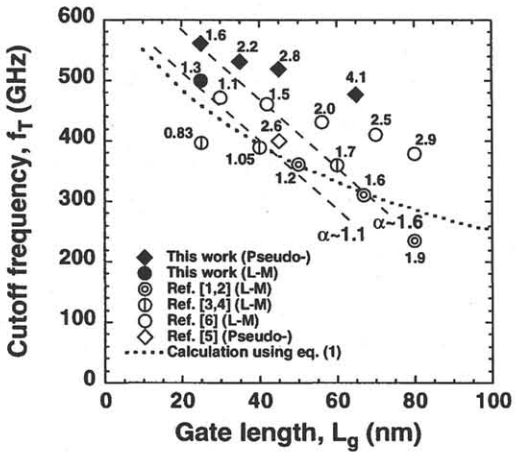

Fig. 3 Gate length L_g dependence of the cutoff frequency f_T in our present and previous works [1-6].

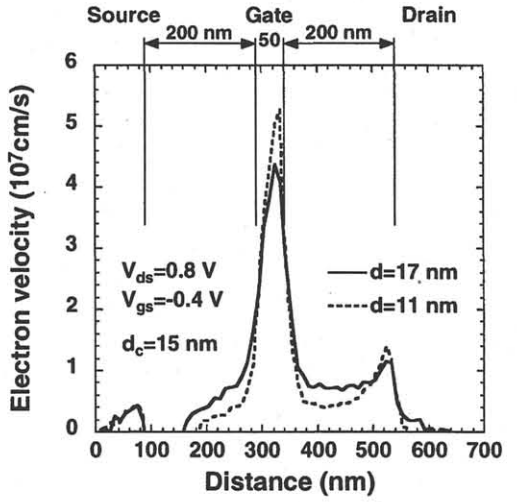

Fig. 4 Electron-velocity profiles in the InGaAs channel of 50-nm-gate lattice-matched HEMTs with $d = 11$ and $d = 17$ nm calculated by using MC simulations.

To clarify the essential origin of the ultrahigh f_T of our HEMTs, we performed Monte Carlo (MC) simulations for the lattice-matched InAlAs/InGaAs HEMTs by using a three-valley model with nonparabolicity. Figure 4 compares two electron-velocity profiles in the InGaAs channel of 50-nm-gate HEMTs with gate-channel distances d of 11 and 17 nm under a V_{ds} of 0.8 V and a V_{gs} of -0.4 V. Under the gate, the electrons are accelerated more quickly at $d = 11$ nm than at $d = 17$ nm. The average electron velocities under the gate are 4.0 x 10^7 and 3.6 x 10^7 cm/s for $d = 11$ and $d = 17$ nm, respectively. A higher electron velocity at $d = 11$ nm is a result of a steeper potential under the gate. Thus, reducing the gate-channel distance enhances the electron velocity, which is consistent with our previous result [6].

4. Summary

In summary, we succeeded in fabricating 25-nm-gate pseudomorphic InAlAs/InGaAs HEMTs with an ultrahigh f_T of 562 GHz by reducing the gate-channel distance. This f_T is the highest value ever reported for any transistor. We also fabricated lattice-matched HEMTs and obtained an f_T of 500 GHz for a 25-nm-gate HEMT, which is superior to the value obtained for a HEMT with a thicker barrier layer. Using MC simulations, we clarified that the ultrahigh f_T of our HEMTs is a result of an enhanced electron velocity under the gate, which in turn is a result of reducing the gate-channel distance.

Acknowledgments

We thank Y. Awano of Fujitsu Laboratories Ltd. for providing the Monte Carlo simulation program. We also thank H. Ohta, N. Hirose, M. Kiyokawa, H. Yasuda, A. Kasamatsu, and M. Higashiwaki of Communications Research Laboratory, T. Kitada and I. Watanabe of Osaka University, and K. Kasai and K. Ikeda of Fujitsu Laboratories Ltd. for their valuable discussions.

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