Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 134-135

G-2-6

Fabrication of Sub-micron Y-Gate InP MESFETs using Crystallographically Defined Contact Technology

Myounghoon Yoon and Kyounghoon Yang

Division of Electrical Engineering
Dept. of Electrical Engineering and Computer Science
Korea Advanced Institute of Science and Technology (KAIST),
373-1 Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea
Phone: +82-42-869-8071 Fax: +82-42-869-8560 E-mail: stage@eeinfo.kaist.ac.kr

1. Introduction

InP-based field effect transistors (FETs) are attractive in high-speed electronic applications [1]. For high-frequency performance of FET devices, a reduction of the device gate length is essential. So far, there have been extensive efforts in making sub-micron T-gate devices using techniques, including the widely used e-beam lithography and novel methods. In order to fabricate T-gate FETs using the e-beam technology, a formation of delicate multilayer photoresist profiles is needed. Recently, there have been reports on formation of sub-micron gate length without using the e-beam lithography by employing special methods, such as micromachined V-grooves [2].

In this work, we propose a new technique of fabricating Y-gate InP MESFETs using a Crystallographically Defined Contact (CDC) technique, which was originally developed for fabrication of self-aligned Emitter-Base HBTs by the authors of this paper [3]. Using the proposed CDC technique based on the conventional optical lithography, a sub-micron Y-shaped gate electrode has been realized. It is found that the fabricated Y-gate device using the proposed CDC technology shows greatly improved overall performance over the conventional devices.

2. Device Structure and Fabrication

The MOCVD grown epitaxial layer structure used in this work is shown in Table 1. The new Y-gate CDC technology utilizes the consistent crystallo-graphic etching characteristics of the dummy InP layer along specific crystal orientations, which can allow highly uniform and precisely controlled sub-micron gate patterning [3]. A double dummy heterostructure, designed to form a sub-micron Y-gate electrode, was grown on top of the conventional InP FET structure. The device fabrication sequence starts with, first, patterning of a gate finger parallel to the $[01\bar{1}]$ crystal direction (primary flat). Then the double dummy layers are etched subsequently using a selective wet etching technique as shown in Fig. 1(a). The consistent crystallographically defined etching profiles with an angle (θ) of 40° are formed for the sub-micron definition. As seen in Fig. 1(a), when a minimum gate dimension of L(1.2μm) is defined using the optical lithography in the contact aligner, the gate-foot dimension on the channel region is reduced down to 0.5μm in our structure from the CDC technique with t=3000Å and θ=40°. Fig. 2 shows the SEM picture of the fabricated sub-micron (L_g=0.5μm) Y-shaped gate electrode. The reduced gate-foot length of 0.5μm agrees well with the designed value. Since the gate-foot length is mainly determined by the crystallographically defined profile of the 1st dummy InP layer in the proposed technology, a more narrow sub-micron Y-shaped gate dimension can be readily realized by adjusting only the thickness of 1st dummy InP layer. The schottky gate metal of Pt/Ti/Pt/Au was evaporated on top of the n⁻ InP channel layer. After the remaining dummy layers contacting the gate electrode are etched by selective wet etching, the sub-micron Y-shaped gate electrode was formed (Fig.1 (b)).

TABLE I
Epitaxial layer structure of fabricated CDC FET

Layer	Material	Thickness (nm)	doping (cm^{-3})
1st dummy	InGaAs	10	undoped
1st dummy	InP	300	undoped
2nd dummy	InGaAs	80	undoped
2nd dummy	InP	25	undoped
Cap	InGaAs	20	$n^{++}= 1 \times 10^{19}$
Cap	InP	10	$n^{+} = 5 \times 10^{18}$
Channel	InP	80	$n^{-} = 4 \times 10^{17}$
Buffer	InP	350	undoped
Substrate	InP		S.I

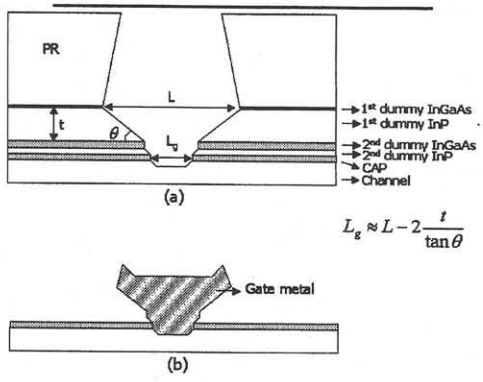

Fig. 1. A brief fabrication sequence of the proposed CDC Y-gate FET

Next, the device was isolated by mesa etching. Then non-alloyed ohmic metal Ti/Au was evaporated on the InGaAs cap layer. The n^{++} InGaAs and n^{+} InP layers existing between the gate and source/drain electrodes were also removed by selective etching. Finally, the devices were ready for measurement by electroplating the interconnect patterns.

3. Measurement and Discussion

Two types of InP MESFETs were fabricated using the optical lithography with a mask set having a minimum gate dimension of $1.2x70\mu m^2$ and source/drain spacing of 5μm. One is fabricated using the CDC technology as discussed in the previous section (CDC-gate FET: L_g=0.5μm), and the other is fabricated using the conventional fabrication method (conventional FET: L_g=1.2μm) after removing the double dummy layers on top of the FET layers. Fig. 3 shows the measured DC characteristics of the fabricated InP MESFETs. Both devices show good pinch-off characteristics. The CDC-gate FET shows a higher saturation current (I_{dss}=6.4mA) than the conventional FET (I_{dss}=4.3mA) at V_{ds}=2V. More than 40% improvement of transconductance (g_m) is obtained for the CDC-gate FET with L_g=0.5μm compared to the conventional devices over the typical gate bias range. The CDC device demonstrated a maximum DC-transconductance of 153mS/mm. The microwave S-parameters of the devices were measured on wafer by using an HP 8720C VNA from 0.5GHz to 18GHz. To find f_T and f_{max}, the current gain h_{21} and Maximum Stable Gain (MSG) were calculated from the measured data and extrapolated by a slope of –20dB/decade. The dependence of cutoff frequencies on the drain current at V_{ds}=2V is shown in Fig. 4. The peak f_t and f_{max} of the CDC–gate FET are 18GHz and 40GHz, and those of the conventional FET are 4.6GHz and 13.9GHz, respectively. The results show that the proposed CDC technique improves high frequency performance of the FETs by more than a factor of three due to the reduced foot dimension of CDC Y-gate. It is expected that the performance of the CDC-gate FET can be further improved by using the source/drain self-aligned ohmic contact technology.

4. Conclusions

A new sub-micron gate-length InP MESFET has been successfully fabricated based on a double dummy heterostructure design using the proposed CDC technology. The maximum cut off frequencies of f_T=18GHz and f_{max}=40GHz were obtained from the device using the conventional optical lithography with a minimum gate patterning dimension of $1.2x70\mu m^2$. The CDC device demonstrated superior performance over the conventional FET devices. By increasing the thickness of the 1st InP dummy layer, further scaling down of the gate foot dimension is expected to be feasible using the proposed technology.

Fig. 2. SEM picture of the fabricated 0.5μm Y-shaped CDC gate

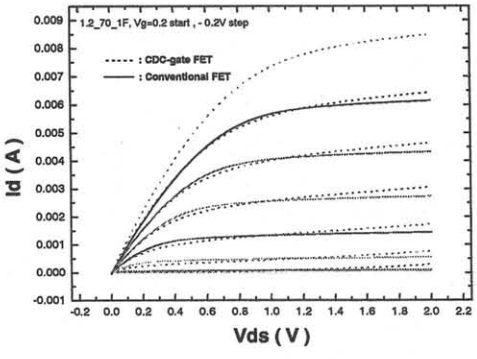

Fig. 3. I-V characteristics of a $1.2x70\mu m^2$ InP MESFET.

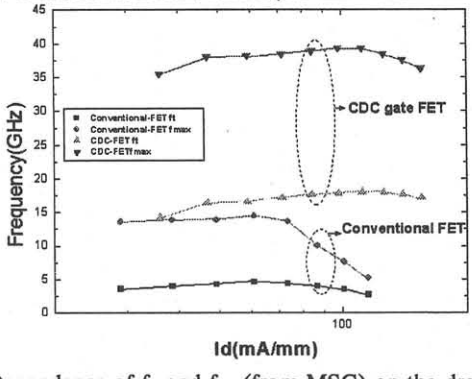

Fig. 4. Dependence of f_T and f_{max}(from MSG) on the drain current of the fabricated InP MESFET at V_{ds}=2V

Acknowledgments

This work was supported by KOSEF under the ERC program through the MINT research center at Dongguk University in Korea.

References

[1] W. Yang et al., 4th Int. Conf. On IEEE IPRM, pp. 368-370, 1992.

[2] H. W. Chiu et al., IEEE EDL, vol.22, no. 9, pp.420-422, Sep., 2001.

[3] M. J. Kim et al., Proc 13th Int. Conf. On IEEE IPRM, pp. 220-223, 2001.