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Impact of SiC Structural Crystal Defects on the Electrical Performance of Bipolar PN Junction Diode

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1. Introduction

Silicon carbide (SiC) technologies for the manufacturing of power devices seem to be promising in the near future. First SiC power devices commercially available are Schottky barrier diodes proposed by Infineon technologies. In the field of switching devices, the current trends are the Accu-MOSFET/ECFET[1] and JFET[2] structures which exhibit the best specific on-resistance experimentally obtained so far. Bipolar power devices stand to benefit greatly in high voltage and high temperature applications. In this work, we present the performance of robust bipolar pn junction devices fabricated on in-house developed high quality 4H-SiC wafers, which are less susceptible to the so called forward current degradation [3].

2. Experimental

To investigate the high density current stress degradation in the bipolar devices, 600V class pn junction diodes were fabricated in 10µm n-type epi-layers grown on n⁺ wafers. Two type of in-house developed 4H-SiC wafers viz., high quality (HQ) and standard (STD) wafers, and a reference wafer were used to evaluate the impact of the SiC structural crystal defects on the electrical performance of the bipolar device. The p-type anode, floating ring edge termination, and n-type field stopper EQR were sequentially implanted with Al and P dopants, respectively to achieve a planar pn junction device structure. Mesh type anode metallization was used to observe the electroluminescence (EL) across the device under the forward bias conditions. The anode active area is about 1.6x10⁻³ cm². The EL images were acquired using the image intensifier module and a CCD camera.

3. Results and Discussion

The forward characteristics of bipolar pn junction diode fabricated on DENSO HQ 4H-SiC wafers is shown in Fig.1. The blue-violet EL from the diode can be observed directly by the naked eyes when the devices are forward biased at elevated current densities. The observed EL result from near-bandgap transitions of free carriers and from free-to-bound recombination of free carriers on shallow dopants. The time-lapse sequence of EL images in the course of degradation of the pn junction diode fabricated on DENSO HO, STD and reference wafers at a stressing current density of about 600A/cm² are shown in Fig.2. The images (a) and (b) were acquired using the image intensifier module at 10µA/cm² and a CCD camera at 600A/cm², respectively. Table I shows the measured etch pit densities of three type of 4H-SiC wafers used in the present degradation analysis. Forward characteristics of degraded pn junction diode fabricated on reference wafer in log and linear scale are shown in Fig.3. Based on the optical and electrical characteristics of the degraded devices, it is possible to speculate about the degradation mechanism. The bright lines observed at low current densities were formed as a result of high current density stress effect. Whereas, these bright lines are viewed as dark features at high current densities and are attributed to a localized reduction of carrier lifetime caused by the creation of extended defects viz., the stacking faults. These created extended defects degrade the device performance due to large recombination current. The defect grows in the direction perpendicular to the offaxis direction and often grows until it span over the whole device area. The nucleation and propagation velocity of defect seems to be different, depending on the quality of the wafers. We observed that defect generation rate is relatively higher for pn junction diodes fabricated on wafer with higher etch pit densities. As evident from Table I that the slip/stacking faults density of in-house developed DENSO HQ wafers is about $1 \sim 2$ order of magnitude lower than that of other wafers used in the present investigations. The continuous SiC material development will eventually lead to the robust bipolar device in the future.

4. Conclusions

We demonstrated that the forward current degradation phenomenon of bipolar pn diodes is strongly related to the SiC structural crystal defects of the starting material.

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References

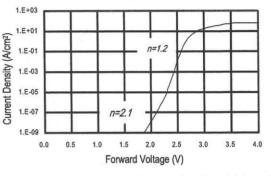
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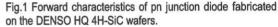
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Table I Measured etch pit densities of 4H-SiC wafers used in the forward current degradation investigation of bipolar pn junction diodes.

4H-SiC	DENSO HQ	DENSO STD	Reference
Defect Type	(1120) off-oriented	(1100) off-oriented	(1120) off-oriented
Etch Pit Density (EPD)	8.0x10 ³ cm ⁻²	1.6x10 ⁵ cm ⁻²	3.2x10 ⁴ cm ⁻²
(i) Micro-pipe Density(ii) Screw Dislocations(iii) Edge Dislocations(iv) Slip/Stacking Faults	0 cm ⁻²	30 cm ⁻²	15 cm ⁻²
	2.9x10 ² cm ⁻²	2.7x10 ⁴ cm ⁻²	6.7x10 ² cm ⁻²
	7.3x10 ³ cm ⁻²	1.1x10 ⁵ cm ⁻²	1.6x10 ⁴ cm ⁻²
	3.8x10 ² cm ⁻²	2.5x10 ⁴ cm ⁻²	1.6x10 ⁴ cm ⁻²



*DENSO HQ and STD stands for the in-house developed high quality and standard wafers, respectively.



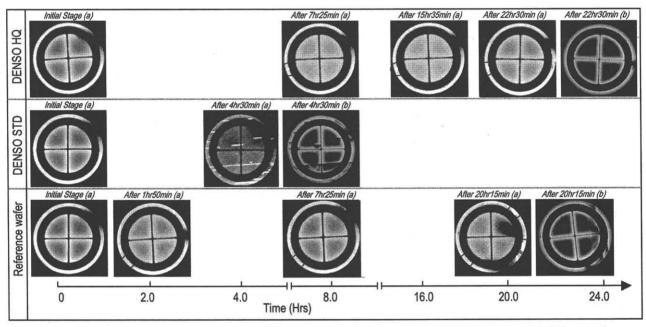


Fig.2 Electroluminescence images in the course of degradation of bipolar pn diode fabricated on DENSO HQ, DENSO STD and reference wafers at a stressing current density of about 600A/cm². The images (a) and (b) were acquired using the image intensifier module and a CCD camera at the current densities of 10µA/cm² and 600A/cm², respectively.

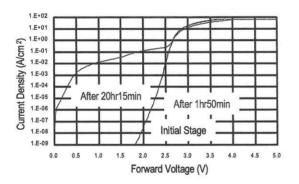


Fig.3(a) Forward characteristics degraded pn junction diode fabricated on reference 4H-SiC wafer (log scale). The created extended defects viz., the stacking faults degrade the pn junction performance due to large recombination current.

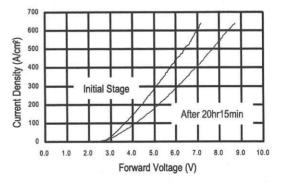


Fig.3(b) Forward characteristics of degraded pn junction diode fabricated on reference 4H-SiC wafer (linear scale). The created stacking fault also causes a drift in the forward voltage (ΔV =1.5V@600A/cm²).