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Analysis of Transconductance Degradation after Endurance Cycling of Uniform F-N Flash Memories

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1. Introduction

We have proposed a 2-Transistor uniform F-N Flash memory for embedding logic LSIs, which utilizes uniform F-N tunneling in both electron injection and emission [1].

This Flash memory requires fast read access even after high endurance cycling, therefore transconductance (Gm) degradation becomes a serious problem.

For Gm degradation, the mechanism has been discussed in Flash memories that utilize CHE in electron injection, and it has already been clarified that the degradation is caused mainly by interface states and trapped electrons located around drain junction edge [2][3]. However, the degradation of a uniform F-N Flash memory has not yet been discussed sufficiently. In this paper, we will analyze Gm degradation induced by uniform F-N tunneling.

2. Experimental

In this study, conventional 1-Transistor uniform F-N Flash memory cells and contacted floating gate cells (FG-cell) are used. Tunnel oxide and effective ONO dielectrics thickness are 11nm and 15nm respectively. The gate length and width are 0.5μm and 0.36μm respectively. Fig.1 shows schematic operation diagrams, and table 1 summarizes the bias conditions.

3. Results and Discussions

Fig.2 shows typical endurance characteristics. Vth window closure is not significant even after high P/E cycles, but Gm degradation becomes very large. In uniform F-N tunneling, it has been known that high endurance cycling generates damages such as interface states and trapped electrons that contribute to Gm degradation [4][5][6].

Fig.3 shows the dependence of Gm degradation on gate stress polarities (±300mA/cm^2) utilizing FG-cells. Larger degradation is observed when gate stress is negative. This result indicates that damages causing Gm degradation are generated mainly in F-N electron emission operation.

To clarify where damages occur in electron emission (channel area, drain junction edge, or gate electrode edge), two experiments have been done.

Fig.4 shows endurance characteristics of two types of gate edge shapes. One is with rounded floating-gate edge, and the other is without. Rounded shapes are formed by Poly-silicon (PS) re-oxidation before LDD ion implantation (I/I). It is found that ΔGm of a cell with PS re-oxidation is suppressed although Vth shifts are similar for two types of gate edge shapes. From this result, it is suggested that its floating-gate edge shape suppresses the electric field concentration around gate edge in F-N electron emission; consequently, the generation of damages is reduced.

Fig.5 shows the dependence on LDD I/I dose ($1x10^{13}$ ~ $1x10^{15}$ cm^{-2}). It is found that Gm degradation is suppressed in the case of higher LDD dose. Here drain junction edge is separated more from gate electrode edge when LDD dose is higher. And if the degradation were caused at drain junction edge like CHE Flash memories, it would not depend either on location of drain junction edge or on LDD dose. But since its dependence is seen actually, it is suggested that damages inducing the degradation are generated mainly not at drain junction edge but at gate electrode edge. Fig.6 shows a schematic representation of the location of damage sites induced by endurance cycling.

Fig.7 shows the device simulation of potential contours in read operation of memory cells of two different LDD dose. In reading a cell of low LDD dose, the depletion region of drain-channel junction is seen on the surface of the substrate under floating-gate edge and Side Wall Spacer. When damages such as interface states and trapped electrons around floating-gate edge overlap the depletion region in read operation, drain voltage drops; read current decreases and it is seen as Gm degradation. On the other hand, in reading cells with high LDD dose, drain voltage does not drop so much because damages do not overlap the depletion region.

4. Conclusions

Transconductance degradation mechanism of uniform F-N Flash memories that utilize uniform F-N tunneling in both electron injection and emission is investigated. It has been clarified that the degradation is caused mainly around the floating-gate electrode edge, which is different from the case of CHE Flash memories. Furthermore, the degradation is mainly caused by interface states and trapped electrons generated in

uniform F-N electron emission, and the damages affect the depletion area around the floating-gate electrode edge in reading operation.

References

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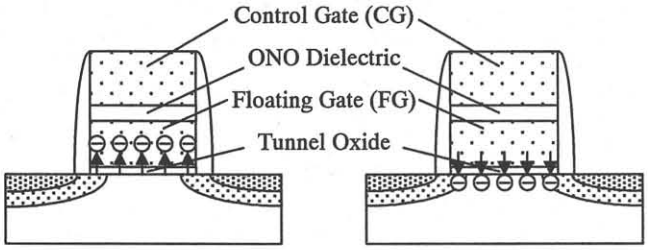
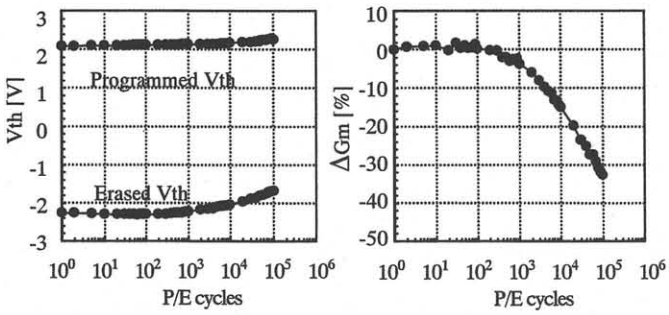


(a) Electron injection. (b) Electron emission

Fig.1 Electron injection and emission by uniform F-N tunneling.

Table 1 Cell operation conditions.

	V_{CG}	V_D	V_S	V_{SUB}	Time
Injection (Program)	15V	0V	0V	0V	10ms
Emission (Erase)	-18V	0V	0V	0V	10ms



(a) Vth.vs.P/E cycles. (b) ΔGm.vs.P/E cycles.

Fig.2 Typical endurance characteristics of a Flash memory utilizing uniform F-N tunneling P/E.

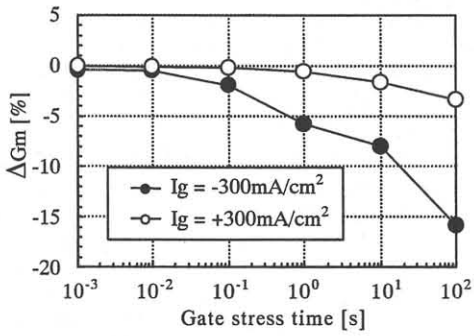
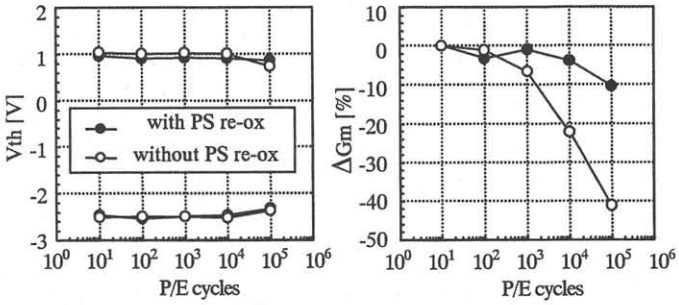
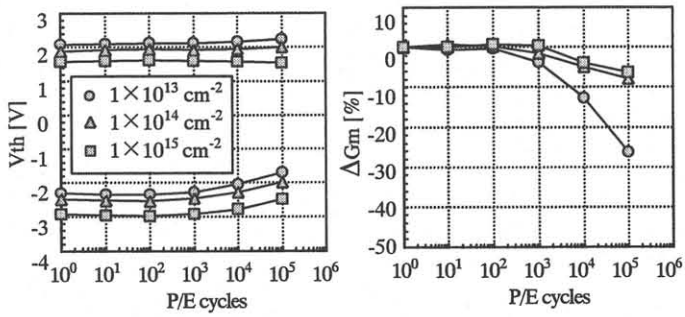


Fig.3 Dependence of gate stress on the polarity.



(a) Vth.vs.P/E cycles. (b) ΔGm.vs.P/E cycles.

Fig.4 Dependence of endurance characteristics on PS re-oxidation (dependence on floating-gate edge shape).



(a) Vth.vs.P/E cycles. (b) ΔGm.vs.P/E cycles.

Fig.5 Dependence of endurance characteristics on LDD dose ($1 \times 10^{13} \sim 1 \times 10^{15}$ cm^{-2}).

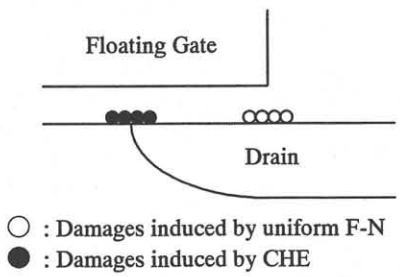
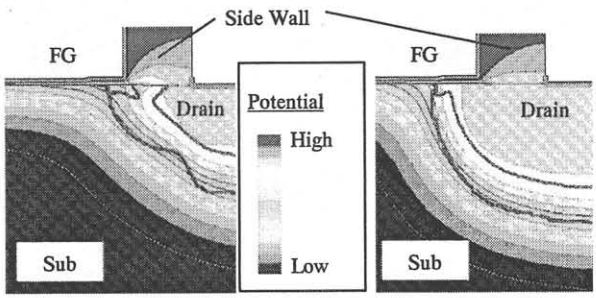


Fig.6 Schematic representation of the location of damages such as interface states and trapped electrons induced by P/E cycling.



(a) Low LDD dose. (b) High LDD dose.

Fig.7 Device simulations of potential contours in reading operation.