

LP10-2

## Transient Behavior of Partially Depleted SOI Non-Volatile Memory Cell and Its Impacts on Device Scaling

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### 1. Introduction

The development of portable electronics spurs the need of high-density embedded non-volatile memory (NVM), and NVM fabricated on SOI is a natural step towards advanced System-On-A-Chip (SOC) applications. However, the commonly used partially depleted (PD) SOI MOSFET is subject to floating body effect that modulation of the threshold voltage ( $V_T$ ) through the body effect [1]. The transient instability in  $V_T$  reduces the noise margin in read operation and increase charge fluctuation in hot electron programming [2]. Such effects are studied in this paper and their impacts to device scaling are examined in detail.

### 2. Device Simulation and Results

The study of the impact of floating body effect on NVM is performed by MEDICI, a two-dimensional device simulator. Two NVM cell structures, one on bulk silicon and one on SOI, are simulated for comparison. The structure of the bulk NVM has a gate length of  $0.35\mu\text{m}$ , gate oxide thickness of 6nm, floating gate thickness of 120nm, and inter-poly oxide thickness of 12nm. The SOI counterpart has similar structures with film thickness is around 200nm that matches the published result of IBM  $0.18\mu\text{m}$  SOI technology node. In programming, the source of the NVM is grounded ( $V_S = 0\text{V}$ ), the drain is biased at  $V_D = 3\text{V}$ . A ramp is applied to the gate that increases from 0V to 9V in 1ns. Figure 1 shows the time domain hot-electron programming current injecting into the floating gate of both SOI and bulk NVM cells. Unlike the bulk NVM cell, a gate current overshoot during the hot-electron programming is observed in the SOI NVM. The amount of overshoot is about 40% of the final current and it takes about 10ns for the overshoot current to settle to the equilibrium value. This overshoot current causes higher charge fluctuation in the floating gate after programming. During read operation, a drain voltage of 0.5V is applied with the gate ramped from 0V to 1.5V in 1ns. The measured drain current ( $I_d$ ) of the SOI NVM, together with the bulk NVM with gate voltage ramped to 1.525V and 1.7V are shown in Figure 2 for comparison. From the figure, the transient floating body effect induce a variation in drain current equivalent to a read voltage fluctuation from 1.7V to 1.525V, causing a loss of 0.175V

in noise margin. It can significantly affect the bit error in determining the state of the memory cell.

The time evolution of body potential under the program and read operations after the gate ramp are shown in figure 3 and figure 4 respectively. After programming, the body potential is maintained at a high voltage that turns on the body-source junction. It helps to remove the excess majority carriers in the body. In reading, the body-source diode is not forward biased enough to remove the carriers stored in the body as shown in figure 4. The excess carriers are thus removed by recombination, which is a slow process and require a much longer time in the order of millisecond to complete.

### 3. Impact on Scaling

Figure 5 shows the settling time in read operation for SOI NVM with different channel length from  $1\mu\text{m}$  down to  $0.3\mu\text{m}$ . With channel length scaling, the transient effect takes longer time to settle and the overshoot current should be used in determining the state of the transistor. However, the settling time of the SOI NVM also depends on the drain current during the read operation as shown in Figure 6. It causes further uncertainty in determining the state of the cell by sensing the drain current. Figure 7 shows the magnitude of the current fluctuation during the read operation at different drain current. Negative values indicate a decreasing current over time (similar to that illustrated in figure 2) and positive values indicate an opposite trend. The increase in drain current is due to impact ionization in the channel at high drain bias which increases the body voltage over time through charging the body-to-source capacitor until it reaches the equilibrium. The interaction between the two opposite behaviors become stronger in short channel NVM cells and make it more difficult to determine the optimal bias and sampling time in read operation.

### 4. Conclusion

The transient floating body effects of PD SOI NVM cell has been studied based. In addition to generating transient instability in read and program, the trend of transient read current evolution is bias and dimension dependent and become more complicated in scaled devices.

### Acknowledgment

This work is supported by a competitive Earmarked Grant HKUST6239/99E from the Research Grant Council of Hong Kong SAR.

### Reference

- [1] Jacque Gautier and Jack Y.-C. Sun, EDL, vol. 16, pp. 497-499, 1995
- [2] Min-Hwa Chi and Albert Bergemont, 1995 SOI Conference, pp. 129-130, 1995

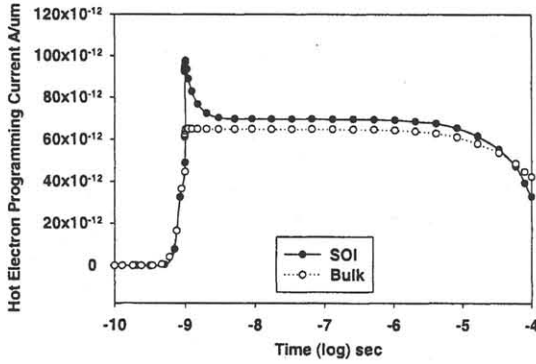


Fig. 1 Hot electron programming current versus time on SOI and Bulk NVM cell

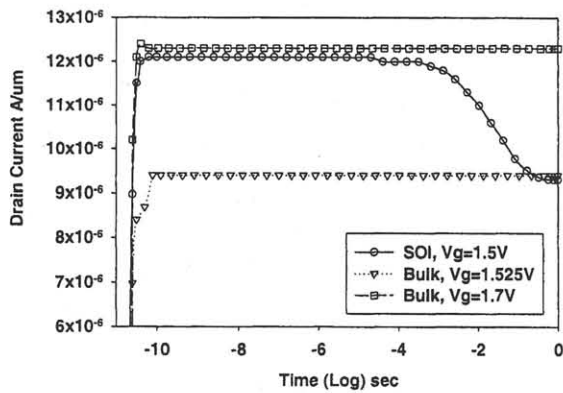


Fig. 2  $I_{\text{drain}}$  in the read operation versus time on SOI and Bulk NVM cell

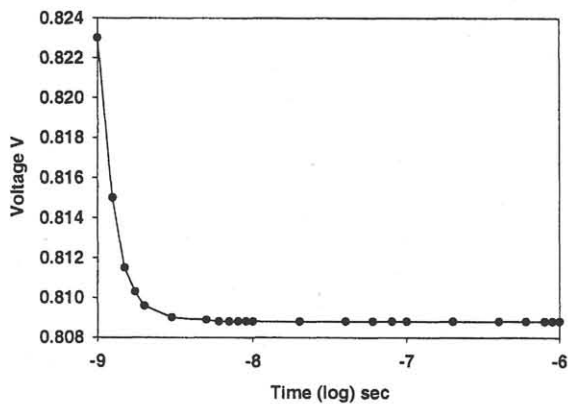


Fig. 3 Body potential of the SOI NVM cell during writing operation

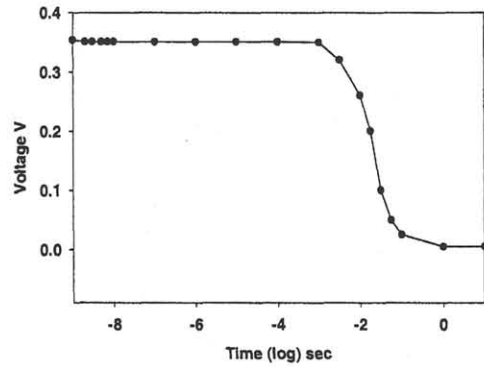


Fig. 4 Body potential of the SOI NVM cell during reading operation

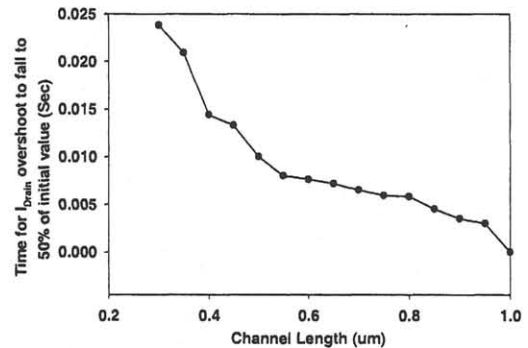


Fig. 5 Transient effect settling time in reading operation versus channel length

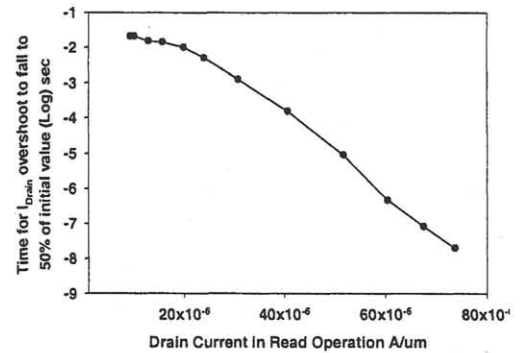


Fig. 6 Transient effect settling time in reading operation versus read current

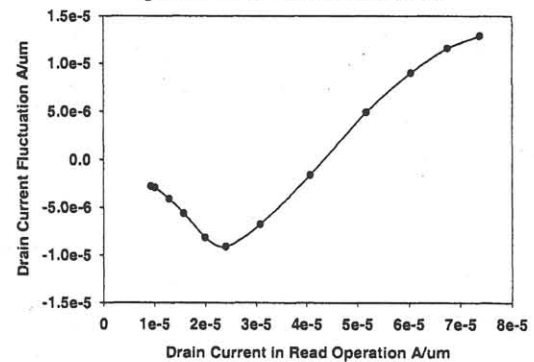


Fig. 7 Read current fluctuation with different read current level