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LP3-2

Sub-10 nm depth ultra low resistance pn junction with antimony implantation

Hiroshi Nakao[1], Kenichi Okabe[2], Tomohiro Kubo[3], Youichi Momiyama[1], and Masataka Kase[3]
Phone: +81-42-532-1252, FAX: +81-42-532-2513, e-mail: hnakao@labs.fujitsu.com
[1] Fujitsu Laboratories LTD. [2] Fujitsu VLSI Process Technology Lab. LTD. [3] Fujitsu LTD.
Fujitsu Akiruno Technology Center, 50 Fuchigami, Akiruno-shi, Tokyo, 197-0833, Japan.

1. Introduction

The scaling of a metal-oxide-semiconductor field-effect-transistor (MOSFET) device for high-end application requires that the junction depth (X_j) be scaled down with the gate length to reduce the short channel effect. Required X_j becomes shallower with the device generation, to be sub-10 nm depth for 45 nm generation on ITRS Road Map[1]. Because of heavy mass and low diffusion constant Sb is suitable for shallow junction. On the other hand, its relatively low solid solubility and tendency to segregate with annealing prevent from device application.

Shibahara et. al.[2] reported that Sb shallow junction for sub-100 nm node transistor is available with controlling dose and annealing condition. In this paper, we demonstrate 7 nm and 10 nm depth junctions are available with low energy antimony implant and annealing technique and examine to adapt as source-drain extension (SDE) for the 90 nm generation transistor.[3]

2. Sb SDE optimization

We used P-type 8" (001)-Si wafers after cleaned with diluted hydrofluoric acid and rinsed with de-ionized water. Sb ions were implanted with acceleration energy of 1 to 8 keV and dose of 5×10^{14} to 1×10^{15} ions/cm^2.

Some wafers are pre-amorphized by germanium (Ge) implant. They were annealed with advanced spike rapid thermal annealing (RTA) technique.

Figure 1 shows Secondary Ion Mass Spectroscopy (SIMS) profiles of as implanted Sb with implant energy 5 keV just along with <001> direction. Because of the heavy mass of Sb ion, atomic stopping is dominant and large channeling tail is observed. This channeling tails is still remained after annealing, whether diffusion occurred or not (fig.2). At higher temperature, surface segregation is emphasized. In this temperature regime, lower R_s is obtained at lower temperature (fig. 3). Lower R_s is also obtained at lower dose at higher temperature (fig. 4). This means too high dose and annealing temperature suppress effective dose, which is caused by deactivation and/or escapement by surface segregation.

Channeling control and low temperature annealing are effective to make an ultra-shallow junction. Figure 5 shows Sb depth profile, pre-amorphized with Ge implant of 20 keV and 5×10^{14} ions/cm^2. 900°C spike annealed profile is also plotted. Pre-amorphization using Ge implant effectively reduced channeling tail of Sb. The X_j of 7.4 and 9.2 nm was obtained.

X_j - R_s plot is shown in figure 6. Data from arsenic (As) implanted sample are also plotted. Sb implanted samples have shallower X_j and lower R_s than As implanted samples in X_j of 7-22 nm regime. The values of X_j = 9.2 nm and R_s = 800 Ω/sq. are satisfy 65 nm node of ITRS road map.

3. Device performance with Sb SDE

We made 90 nm node MOSFET using this Sb SDE with L_g of 45 nm. Figure 7 shows SDE dose dependence on overlap capacitance (C_{ov}) and SDE resistance (R_{ext}). C_{ov} saturation and R_{ext} increase for higher SDE dose were observed, the same as fig. 4 case. At higher dose range, excess Sb atoms enhance deactivation of super-saturated Sb dopant and suppressing effective dose. I_{on} current also has optimum SDE dose (fig. 8). In low dose range, C_{ov} is not enough to get high I_{on} current, too high dose decreases I_{on} current due to increasing R_{SDE}. Maximum I_{on} of 840 μA/um is obtained at I_{off} of 0.1 μA/um.

4. Summary

We demonstrate Sb ultra-shallow junction for 65 nm node transistor using low energy implant and RTA technique. The 90 nm node transistor with Sb SDE shows good performance in L_g of 45 nm.

References

1. ITRS2001-FEP; The International Technology Roadmap for Semiconductors, Dec 2001 (Ed. International SEMATECH)
2. K. Shibahara, K. Egusa, K. Kamesaki and H. Furumoto, Jpn. J. Appl. Phys. **39** (2000) 2194.
3. S. Nakai et al., Proc. of 2002 SYMPOSIUM ON VLSI TECHNOLOGY. (2002) 66.

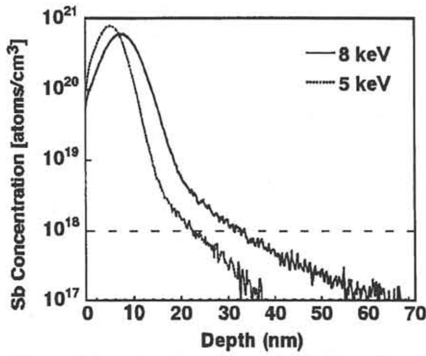

Fig. 1: SIMS profile of as implanted Sb into Si crystal from 0° incident. Large channeling tail is observed.

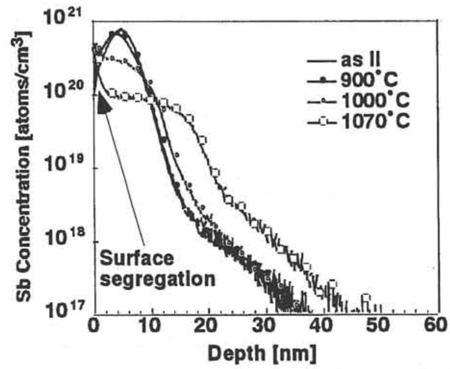

Fig. 2: Annealing temperature dependence of 5 keV Sb profile of the samples of fig.1.

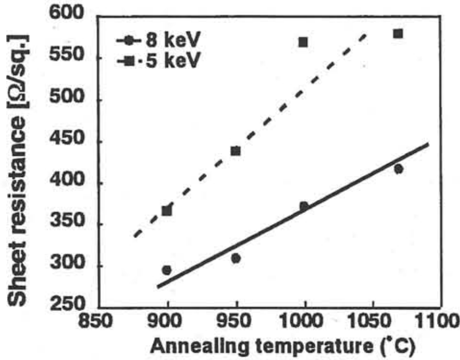

Fig. 3: Sheet resistance vs. annealing temperature. Sheet resistance is increased with annealing temperature.

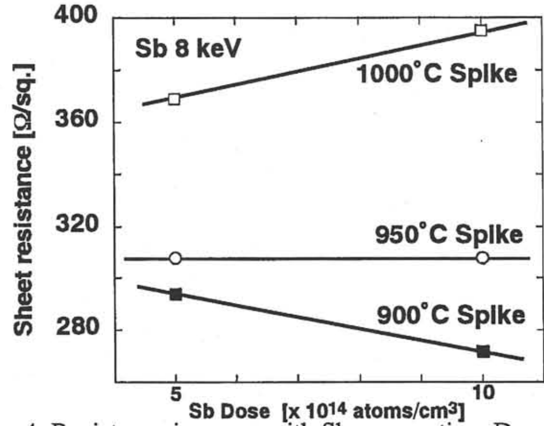

Fig. 4: Resistance increase with Sb segregation. Deactivation observed at high temperature.

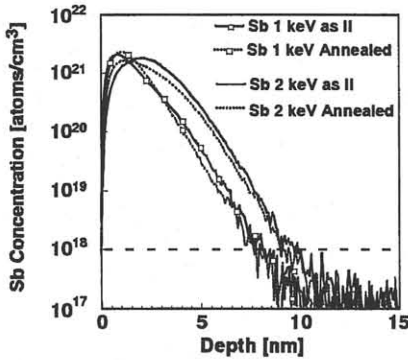

Fig. 5: Ultra-shallow junction with Sb dopant with ge pre-amorphization. Xj 9.2 and 7.4 nm is obtained.

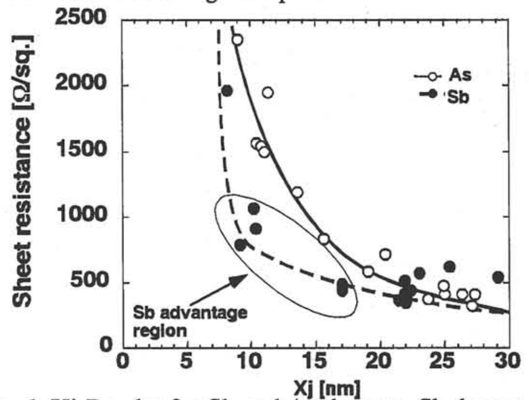

Fig. 6: Xj-Rs plot for Sb and As dopant. Sb dopant have lower resistance in ultra-shallow junction.

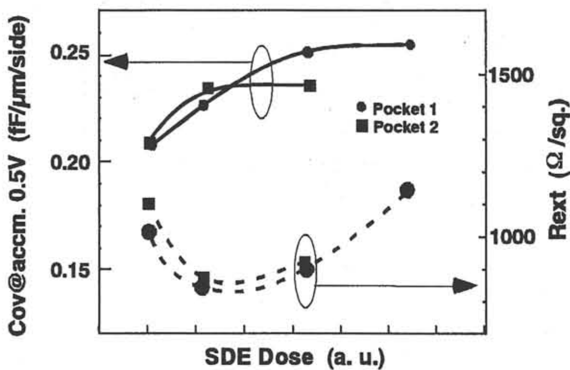

Fig. 7: C_{ov} and R_{ext} vs. SDE dose. C_{ov} saturation and R_{ext} increase is observed in higher dose.

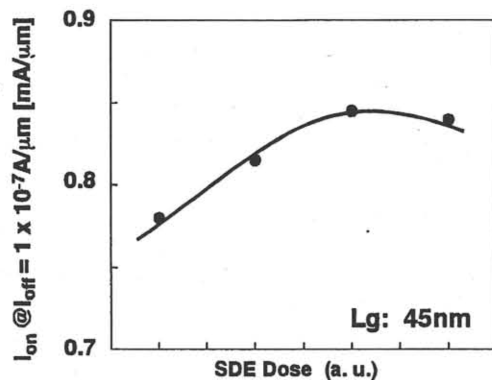

Fig. 8: SDE dose vs. I_{on} current. Optimum dose are obtained.