Characterization of traps at SOI/BOX interface 
by back gate transconductance characteristics in SOI MOSFETs


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1. Introduction

It has been pointed out that trap states in SOI layers have significant influence on the electrical characteristics of devices fabricated on SOI wafers [1]. It has also been shown that the subthreshold slope of SOI MOSFET is increased by trap states at SOI/BOX interface [2]. On the other hand, we have demonstrated that SOI MOSFETs by full inversion which have ultra thin SOI layers less than 10 nm is effective to suppress short channel effect in deep sub-micron gate MOSFETs [3], and then the characterization and control of trap state at SOI/BOX interface will be more critical to fabricate ultra thin SOI MOSFETs with practical use. However, it cannot be said that traps in SOI layers has been investigated in detail. Therefore in this study we will try to characterize traps in SOI layers by analyzing the electrical characteristics of MOSFETs.

2. Experiments and Device simulations

ELTRAN wafers and low-dose SIMOX wafers fabricated using ITOX process were used as SOI wafers. And two kinds of SOI MOSFETs were fabricated as shown in Fig. 1 and Fig. 4: one is normally-on type n-channel MOSFETs fabricated on a p-type SOI substrate and the other is normally-on type p-channel MOSFETs fabricated on a p-type SOI substrate. From n-channel MOSFETs, majority carriers of Ip are electrons in inversion layer, while in p-channel MOSFETs, majority carriers of Ip are holes and Ip is controlled by the spread of depletion layer. The characteristics of drain current Ip-back gate bias Vo were measured at the configuration as shown in Fig. 2 and Fig. 5. The device simulation of these SOI MOSFETs was performed by 3-dimensional drift-diffusion device simulator, in which traps and recombination rates were assumed to be the same as in bulk Si.

3. Results and discussions

Figure 2 and Figure 5 show Ip-Voa characteristics of n-channel and p-channel SOI MOSFETs, respectively. Figure 3 and Figure 6 show gm-Voa characteristics obtained from Fig. 2 and Fig. 5, respectively.

Figure 3 illustrates that the dip of gm appears, even in low-dose SIMOX (ITOX) wafers, while the dip at gms-Voa characteristics was also observed in SOI MOSFETs using high-dose SIMOX wafers which were expected to have many traps [4]. Figure 6 demonstrates that the dip of gm appears also in p-channel depletion layer controlled FETs in low-dose SIMOX (ITOX) wafers, though they have smooth SOI/BOX interfaces.

From the back gate gm characteristics, the trap density can be simply formulated by eq. (1)

\[ N_T(W_S) = \frac{C_{ox}}{q} \frac{dI_P}{dW_S} \left( \frac{1}{g_{m,exp}} - \frac{1}{g_{m,ann}} \right) \]  

, where C_{ox} is the capacitance of BOX, W_S is surface potential at SOI/BOX interface, W is gate width and g_{m,exp} and g_{m,ann} refer to transconductance gm obtained by experiments and device simulations, respectively. dI_P/dW_S in eq. (1) is obtained by the device simulation.

As a result, traps density at SOI/BOX interface was estimated to be less than 10^{11} (cm^{-2}eV^{-1}) in ELTRAN wafers. On the other hand, in low-dose SIMOX (ITOX) wafers, it was estimated to be more than 10^{12} (cm^{-2}eV^{-1}).

Figure 7 shows the distribution of traps density at SOI/BOX interface in low-dose SIMOX (ITOX) wafers. In Fig. 7, two bands of trap states are obtained: a narrow band with the density of 5x10^{11} (cm^{-2}eV^{-1}) is obtained at ∼0.4 (eV) above the Si midgap Ei from the large sharp dip of gm in n-channel FETs as shown in Fig. 3, and a broad band with the density of 10^{12} (cm^{-2}eV^{-1}) is obtained at 0.3-0.4 (eV) below Ei from the small kink of gm in p-channel FETs as shown in Fig. 6. It is note that the extra shift of Vo of Ip-Vo curve at SIMOX from that at ELTRAN is positive in Fig. 2 and negative in Fig. 5. Therefore we concluded that a narrow band above Ei is "acceptor-like electron traps" and a broad band above Ei is "donor-like hole traps".

4. Conclusion

We characterized trap density at SOI/BOX interfaces by adopting our very simple analytical formula to n-channel MOSFETs and to p-channel depletion layer-controlled MOSFETs. As a result, we found that it is less than 10^{11} (cm^{-2}eV^{-1}) in ELTRAN wafers, while even in low-dose SIMOX (ITOX) wafers, whose trap density is believed to be lower than that of high-dose SIMOX wafers, "accepter-like electron traps" with the density of 5x10^{11} (cm^{-2}eV^{-1}) near Ei and "donor-like hole traps" with the density of 10^{11} (cm^{-2}eV^{-1}) near Ei are distributed.

This approach is effective to characterize and control of traps at SOI/BOX interfaces, which will have more influence on electrical characteristics of SOI devices significantly.

Reference
Fig. 1: A schematic view of n-ch SOI MOSFET

Fig. 2: $I_D-V_{BG}$ characteristics of n-ch SOI MOSFET

Fig. 3: $g_m-V_{BG}$ characteristics of n-ch SOI MOSFET

Table 1: Typical parameters of FETs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Length</td>
<td>50 (µm)</td>
</tr>
<tr>
<td>Gate Width</td>
<td>50 (µm)</td>
</tr>
<tr>
<td>FOX</td>
<td>n-ch 23 (nm)</td>
</tr>
<tr>
<td>SOI</td>
<td>50 (nm)</td>
</tr>
<tr>
<td>BOX</td>
<td>100 (nm)</td>
</tr>
</tbody>
</table>

Fig. 4: A schematic view of p-ch SOI MOSFET

Fig. 5: $I_D-V_{BG}$ characteristics of p-ch SOI MOSFET

Fig. 6: $g_m-V_{BG}$ characteristics of p-ch SOI MOSFET

Fig. 7: Energy distribution of interface trap density in forbidden gap of Si at SOI/BOX interface in low-dose SIMOX (ITOX) wafers