Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 604-605

LP9-1

Characterization of traps at SOI/BOX interface by back gate transconductance characteristics in SOI MOSFETs

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1. Introduction

It has been pointed out that trap states in SOI layers have significant influence on the electrical characteristics of devices fabricated on SOI wafers [1]. It has been also shown that the subthreshold slope of SOI MOSFET is increased by trap states at SOI/BOX interface [2]. On the other hand, we have demonstrated that SOI MOSFETs by full inversion which have ultra thin SOI layers less than 10 (nm) is effective to suppress short channel effect in deep sub-micron gate MOSFETs [3], and then the characterization and control of trap state at SOI/BOX interface will be more critical to fabricate ultra thin SOI MOSFETs with practical use. However, it cannot be said that traps in SOI layers has been investigated in detail. Therefore in this study we will try to characterize traps in SOI layers by analyzing the electrical characteristics of MOSFETs.

2. Experiments and Device simulations

ELTRAN wafers and low-dose SIMOX wafers fabricated using ITOX process were used as SOI wafers. And two kinds of SOI MOSFETs were fabricated as shown in Fig. 1 and Fig. 4: one is normally-off type n-channel MOSFETs fabricated on a p-type SOI substrate and the other is normally-on type p-channel MOSFETs fabricated on a p-type SOI substrate. In n-channel FETs, majority carriers of I_D are electrons in inversion layer, while in p-channel FETs, majority carriers of I_D are holes and I_D is controlled by the spread of depletion layer. The characteristics of drain current I_D-back gate bias V_{BG} were measured at the configuration as shown in Fig. 2 and Fig. 5. The device simulation of these SOI MOSFETs was performed by 3-dimensional drift-diffusion device simulator, in which traps and recombination rates were assumed to be the same as in bulk Si.

3. Results and discussions

Figure 2 and Figure 5 show I_D-V_{BG} characteristics of n-channel and p-channel SOI MOSFETs, respectively. Figure 3 and Figure 6 show g_m-V_{BG} characteristics obtained from Fig.2 and Fig.5, respectively.

Figure 3 illustrates that the dip of g_m appears, even in low-dose SIMOX (ITOX) wafers, while the dip at g_m-V_{BG} characteristics was also observed in SOI MOSFETs using high-dose SIMOX wafers which were expected to have many traps [4]. Fig.6 demonstrates that the dip of g_m appears also in p-channel depletion layer controlled FETs in low-dose SIMOX (ITOX) wafers, though they have smooth SOI/BOX interfaces.

From the back gate g_m characteristics, the trap density can be simply formulated by eq. (1)

$$N_{SS}(\psi_S)=\frac{1}{q}\cdot\frac{C_{OX}}{W}\cdot\frac{dI_D}{d\psi_S}\cdot\left(\frac{1}{g_m^{\,exp.}}-\frac{1}{g_m^{\,sim.}}\right) \quad (1)$$

, where C_{OX} is the capacitance of BOX, ψ_s is surface potential at SOI/BOX interface, W is gate width and $g_m^{exp.}$ and $g_m^{sim.}$ refer to transconductance g_m obtained by experiments and device simulations, respectively. $\frac{dI_D}{d\psi_S}$ in eq. (1) is obtained by the device simulation.

As a result, traps density at SOI/BOX interface was estimated to be less than 10^{11} ($cm^{-2}\cdot eV^{-1}$) in ELTRAN wafers. On the other hands, in low-dose SIMOX (ITOX) wafers, it was estimated to be more than 10^{12} ($cm^{-2}\cdot eV^{-1}$).

Figure 7 shows the distribution of traps density at SOI/BOX interface in low-dose SIMOX (ITOX) wafers. In Fig.7, two bands of trap states are obtained: a narrow band with the density of 5×10^{12} ($cm^{-1}eV^{-1}$) is obtained at ~0.4 (eV) above the Si midgap E_i from the large sharp dip of g_m in n-channel FETs as shown in Fig.3, and a broad band with the density of 10^{12} ($cm^{-1}eV^{-1}$) is obtained at 0.3~0.4 (eV) below E_i from the small kink of g_m in p-channel FETs as shown in Fig.6. It is note that the extra shift of V_{BG} of I_D-V_{BG} curve at SIMOX from that at ELTRAN is positive in Fig.2 and negative in Fig.5. Therefore we concluded that a narrow band above E_i is "accepter-like electron traps" and a broad band above E_i is "donor-like hole traps".

4.Conclusion

We characterized trap density at SOI/BOX interfaces by adopting our very simple analytical formula to n-channel MOSFETs and to p-channel depletion layer-controlled MOSFETs. As a result, we found that it is less than 10^{11} ($cm^{-1}eV^{-1}$) in ELTRAN wafers, while even in low-dose SIMOX (ITOX) wafers, whose trap density is believed to be lower than that of high-dose SIMOX wafers, "accepter-like electron traps" with the density of 5×10^{12} ($cm^{-1}eV^{-1}$) near E_c and "donor-like hole traps" with the density of 10^{12} ($cm^{-1}eV^{-1}$) near E_v are distributed.

This approach is effective to characterize and control of traps at SOI/BOX interfaces, which will have more influence on electrical characteristics of SOI devices significantly.

Reference

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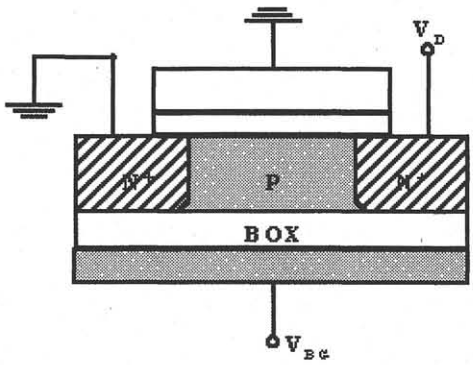

Fig.1: A schematic view of n-ch SOI MOSFET

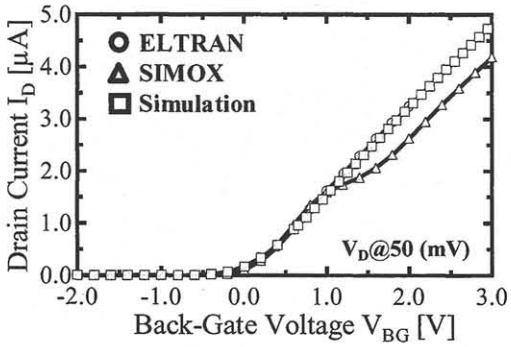

Fig.2: I_D-V_{BG} characteristics of n-ch SOI MOSFET

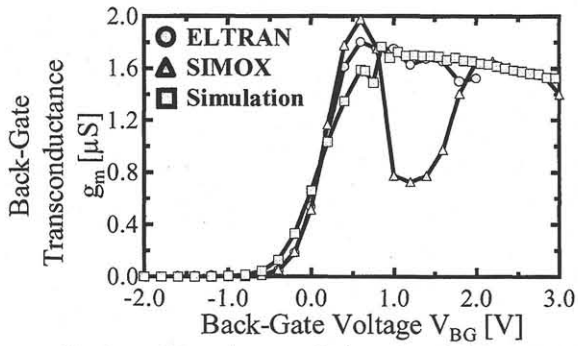

Fig.3: g_m-V_{BG} characteristics of n-ch SOI MOSFET

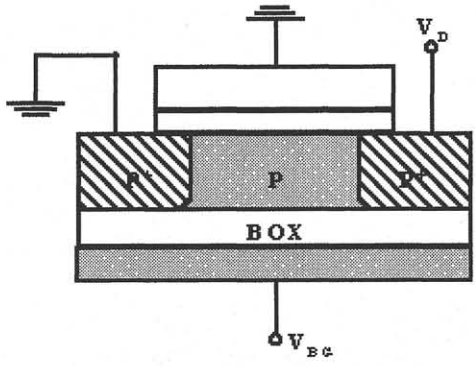

Fig.4: A schematic view of p-ch SOI MOSFET

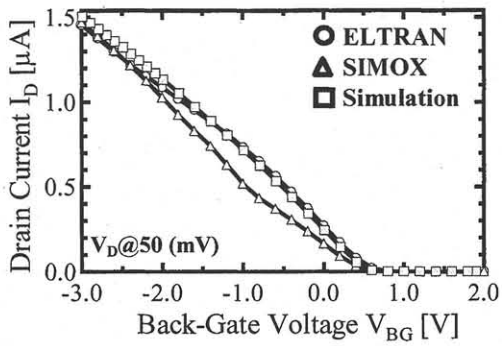

Fig.5: I_D-V_{BG} characteristics of p-ch SOI MOSFET

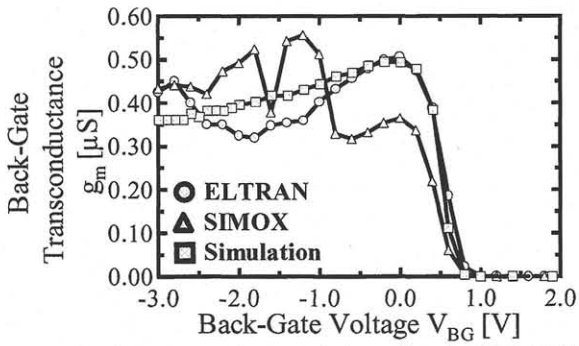

Fig.6: g_m-V_{BG} characteristics of p-ch SOI MOSFET

Table I Typical parameters of FETs

Gate Length	50 (μm)
Gate Width	50 (μm)
FOX	n-ch 23 (nm) p-ch 100 (nm)
SOI	50 (nm)
BOX	100 (nm)

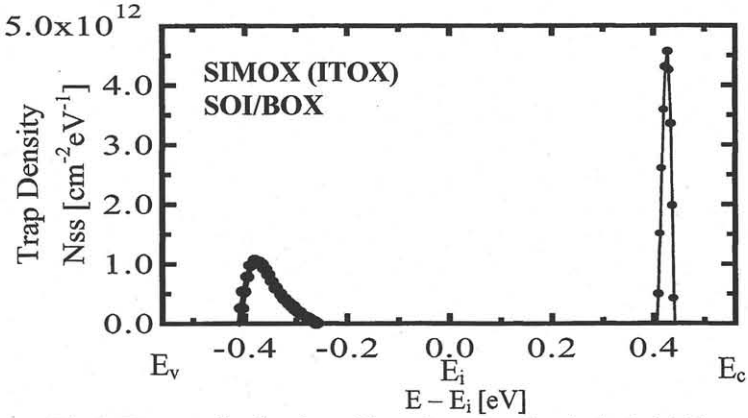

Fig.7: Energy distribution of interface trap densityin forbidden gap of Si at SOI/BOX interface in low-dose SIMOX (ITOX) wafers