Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 370-371

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A 10-GHz Bipolar VCO with Reduced Phase Noise

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1. Introduction

In high-speed communication systems and high-frequency measurement systems, the high-performance voltage-controlled oscillators (VCOs) are required. Especially, high frequency operation beyond 10GHz and reduction of phase noise at close-to-carrier frequency become important.

Not only studies of high-speed and low-noise devices and high-Q on-chip inductors, but also circuit design technology are required. This paper proposes a circuit design technology to reduce phase noise by optimizing operating point.

2. Phase Noise in LC Oscillators

The phase noise in LC oscillators $\mathcal{L}(\Delta\omega)$ is given by Eq. 1 [1, 2]

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left[\frac{4FkT}{A^2 G_L} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \quad \text{[dBc/Hz]} \quad (1)$$

where F is an empirical parameter (often called the "device excess noise number"), k is Boltzmann's constant, T is the absolute temperature, A is the oscillation amplitude, G_L is the parallel parasitic conductance of the resonator, ω_0 is the carrier frequency, Q is the quality factor of the resonator, and $\Delta\omega$ is the frequency offset. In order to reduce the phase noise, we use a high-Q inductor and maximize the oscillation amplitude. In the GHz VCO, usually inductors are formed on the chip, and its Q is limited to less than 10. Therefore, this paper describes optimizing technique of oscillation amplitude.

3. Phase Noise Reduction by Optimization of the Operating Point

The oscillation amplitude of the VCO in Fig. 1 is determined by $L \cdot di/dt$. Assuming L is fixed, we can understand that the way to maximize amplitude is to increase the currents. But, amplitude is saturated and phase noise becomes worse when currents are increased beyond the point of X as shown in Fig. 2. In this case, Q_1 and Q_2 operate in the saturation region momentarily. The operating point of the transistor must be optimized to decrease the phase noise. Ideally, a transistor is designed to operate in the active region completely, and we must increase amplitude to the full range surrounded in breakdown and saturation voltages.

As shown in the DC-coupled VCO of Fig. 1(a), a feedback DC level from the collector of Q_1 is shifted by the emitter follower Q_7 and is then added to the base of Q_2 to avoid a saturation region. By this technique, the operating period in the saturation region certainly can be reduced, but the oscillation waveform is distorted as shown in Fig. 3(a). This phenomenon occurs because there is a moment when a transistor operates in the saturation region, and it can be confirmed from the operating point loci, as shown in Fig. 4(a).

To overcome this problem, AC-coupled VCO, as shown in Fig. 1(b), is proposed. This circuit can cut the DC signal of the feedback path and give the proper base bias current. By using this circuit, we enlarged the transistor in order to lower the saturation voltage, and optimized an operating point based on the theory stated above. As a result, a transistor always operated in the active region, as shown in Fig. 4(b). The oscillation waveform is close to the sinusoid as shown in Fig. 3(b), and it maximized amplitude with low distortion to 2.3Vp-p.

Figure 5 shows simulated phase noise with SpectreRF. The phase noise at 100kHz offset of the AC-coupled VCO is 10dBc/Hz lower than the DC-coupled VCO.

4. Chip Fabrication and Measurement Results

We designed a 10GHz VCO by using silicon bipolar technology with f_T=45GHz. The measured Q of the inductor is about 6 at 10GHz. Figure 6 shows a micrograph of the VCO test chip. The measured frequency-tuning curve is shown in Fig. 7. The VCO oscillates from 9.5GHz to 11.3GHz. Figure 8 shows the measured phase noise. The phase noise at 100kHz offset from 10.4GHz carrier is -80dBc/Hz. This value is 5dBc/Hz higher than the simulation results. We estimated this degradation is caused by the noise at tuning node and power supply node of the VCO.

5. Conclusion

We successfully designed and fabricated a 10GHz VCO by using silicon bipolar technology. The phase noise was reduced to -80dBc/Hz at 100kHz offset from 10GHz carrier by optimizing the operating point of the transistor.

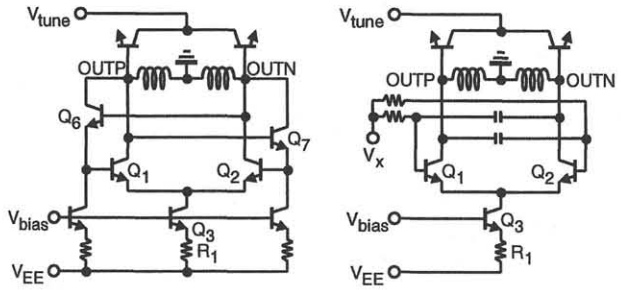

Fig. 1: (a) DC-coupled VCO, and (b) AC-coupled VCO.

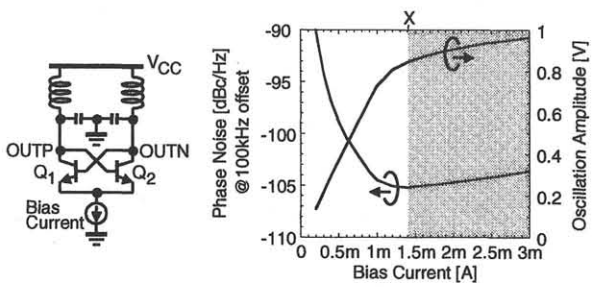

Fig. 2: Bias-current dependence of amplitude and phase noise.

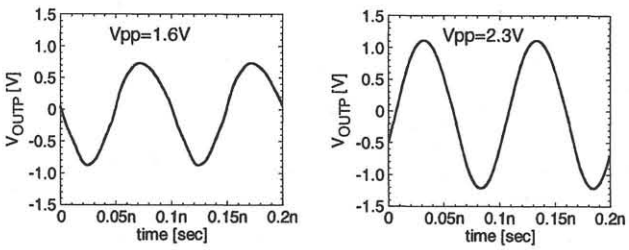

Fig. 3: The oscillation waveforms at node OUTP of (a) DC-coupled VCO, and (b) AC-coupled VCO.

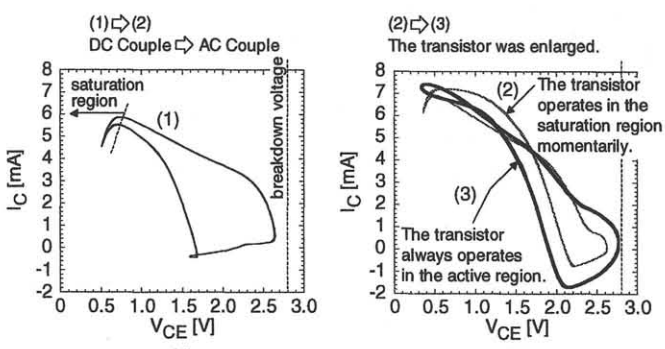

Fig. 4: Operating point loci of (a) DC-coupled VCO, and (b) AC-coupled VCO.

References

[1] D. B. Leeson, *Proc. IEEE*, 329-330 (1966).

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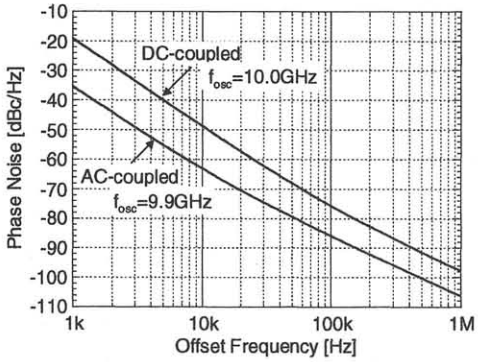

Fig. 5: Simulated phase noise with SpectreRF.

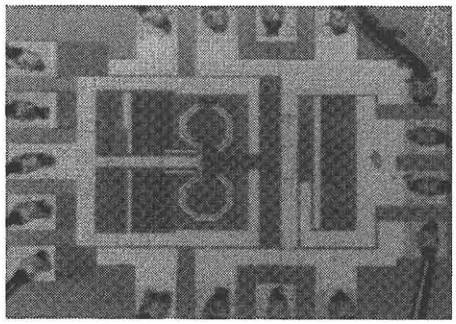

Fig. 6: Micrograph of the VCO test chip.

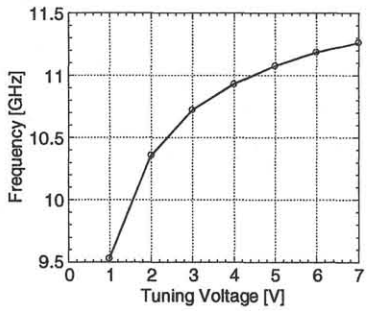

Fig. 7: Measured frequency-tuning curve of the AC-coupled VCO.

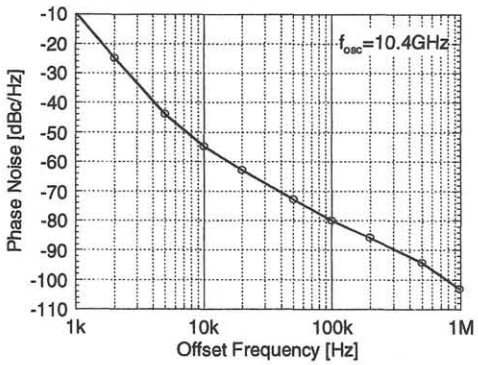

Fig. 8: Measured phase noise of the AC-coupled VCO.