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A High-Resolution Hadamard Transform Chip

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1. Introduction

An artificial retina chip, capable of edge detection and projection, was proposed in an earlier paper [1]. However, in order to apply that chip to machine vision, high-order feature extraction is required. We then proposed a chip that had a Hadamard transform function, which is an orthogonal transformation function [2].

However, two big capacitors were required in each pixel of this Hadamard transform chip, because of the optical-electric (O-E) conversion and the charge sharing addition. Since the pixel area was large, the resolution was limited to 64x64 pixels in 4.73mm^2. On the other hand, a resolution of at least 200x200 pixels is required to enable machine vision to treat two or more objects.

We therefore propose a new high-resolution Hadamard transform circuit that does not require capacitors in the pixels. The capacitors that were required for O-E conversion become unnecessary, because the proposed system uses photo detector (PD) current directly, without converting it into pulse width. When the current addition is used, the parasitic capacitor of a common line becomes a problem; this problem is solved by stabilization of the common line and charge packet counting (CPC) technique [3].

2. Hadamard Transform Circuit

Figure 1 (top) shows a Hadamard transform circuit. The Hadamard transform circuit is composed of two base generators, a pixel array, and two CPCs.

Each base generator is composed of a one-dimensional Hadamard base generator and shift register. These generators, located on the row side and column side, provide three states (+1, -1, 0) to each pixel. Table I shows how the +1, -1 and 0 states are coded.

Table I: Tri-state coding in pixel

	ROW	$\overline{\text{ROW}}$		COL	$\overline{\text{COL}}$	PLUS	MINUS
+1	LO	HI	+1	LO	HI	i_{PD}	HiZ
+1	LO	HI	−1	HI	LO	HiZ	i_{PD}
−1	HI	LO	+1	LO	HI	HiZ	i_{PD}
−1	HI	LO	−1	HI	LO	i_{PD}	HiZ
0	HI	HI		any		HiZ	HiZ
	any		0	HI	HI	HiZ	HiZ

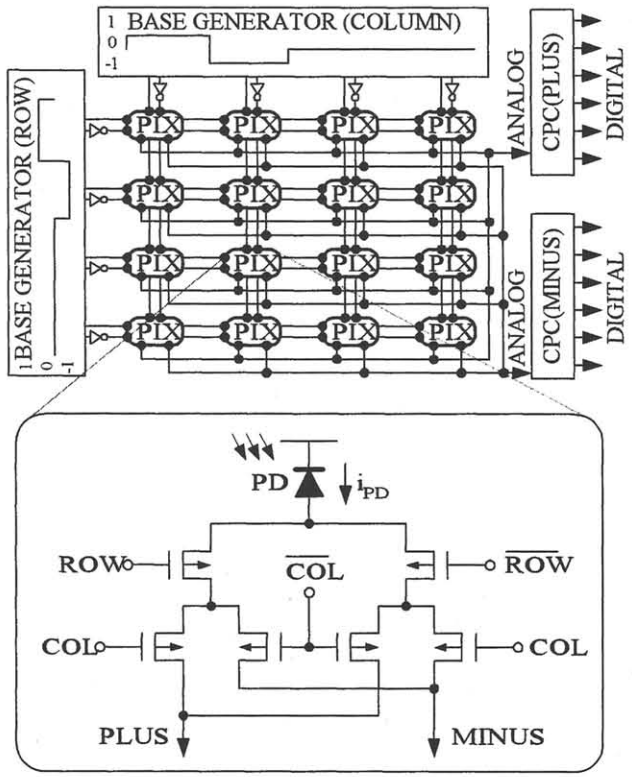

Fig. 1 Block diagram of Hadamard transform circuit

Each pixel consists of a PD and a four-quadrant multiplier. The PD outputs current in proportion to optical intensity. The current is shunted to either the PLUS or MINUS terminal, depending on the state of ROW and that of COL:

$$i_{PLUS} - i_{MINUS} = i_{PD}\left(ROW - \overline{ROW}\right)\left(COL - \overline{COL}\right) \quad (1)$$

The artificial retina chip also supplies the three states to pixels in similar ways. However, it is not able to perform the spatial orthogonal transformation because the supply is from the column only and because each pixel is only a two-quadrant multiplier.

The PLUS and MINUS terminals are connected to a common line respectively, and current addition is carried out.

This addition was realized by using charge sharing. Also, the capacitors had to be large enough to accommodate parasitic capacitance. With the proposed circuit, however, this capacity becomes unnecessary by the current addition.

The CPC circuit (Fig. 2) has two functions. One is analog-to-digital conversion. The other is a virtual elimination of a common line's parasitic capacitor, which is a big problem with current addition. The digital value is obtained by counting the pulse of the current-controlled oscillator. The parasitic capacitor is eliminated by an imaginary short.

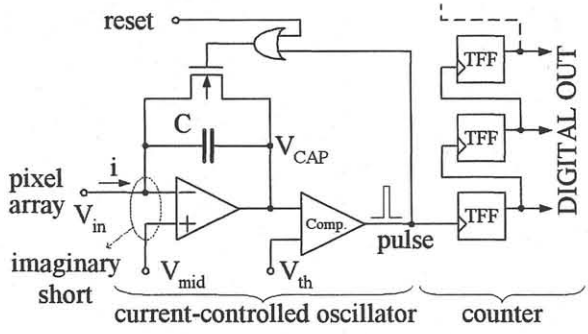

Fig. 2 Charge packet counting circuit

Since a dynamic range is the ratio of an input i, it will be decided by Eq. 2.

$$i_{max}/i_{min} = \frac{V_{max}C}{t_{min}} \Big/ \frac{V_{min}C}{t_{max}} = f_{max}V_{max}/f_{min}V_{min} \qquad (2)$$

Where, t_{min} is the minimum pulse interval restricted to time of discharging C, t_{max} is the maximum period of A/D converting and, f_{max} and f_{min} are the oscillator's frequency, which are equal to inverse of t_{min} and t_{max}. The threshold voltage V_{th} is changed from V_{max} to V_{min} depending on the amount of current i. (See also Fig. 3)

The dynamic range was estimated at 55.6[dB] by Eq. 2. (fmax=1MHz, fmin=10kHz, Vmax=0.6V, Vmin=0.1V)

3. Chip Design

In consideration of parasitic capacitance, the behavior of the current is changed into pulse as simulated by SPICE (Fig. 3).

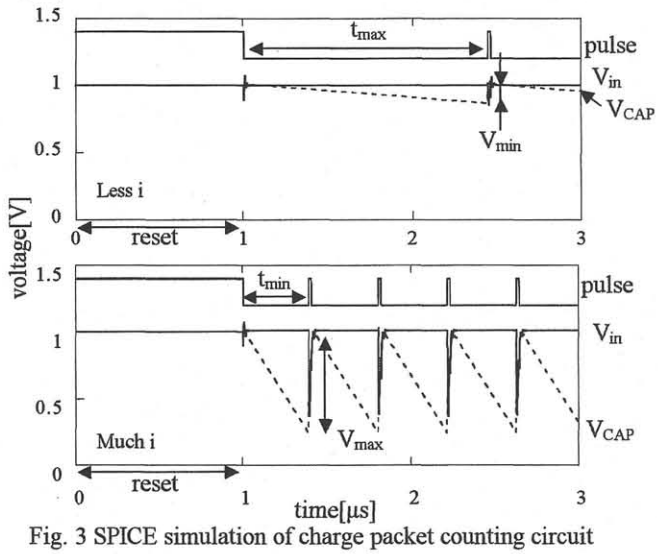

Fig. 3 SPICE simulation of charge packet counting circuit

The capacitor voltage V_{CAP} is reset at first, and it decreases depending on the current i. When the voltage reaches the threshold V_{th}, the pulse is generated and the voltage is reset. The voltage stabilization of input terminal by voltage feedback is confirmed.

The test chip was designed with a 0.35μm CMOS process on three-layer aluminum and two-layer poly. The chip layout is shown in Fig. 4. As explained in section 2, it consists of two base generators, a pixel array, and two CPCs. A pixel is magnified and shown in part of Fig. 4.

Each pixel is made of six PMOSs and a PD. Since these are made in the same n-well, the requisite area can be minimized. Since only positive power (VDD) was required for the power supply, the power line was shared with the mask for shading (third metal layer). With these optimizations, one pixel can be realized in 14.4μm^2 leaving 42% of the photo detection area open. The base generator and the CPC can be realized compactly. As a result, 256 x 256 pixels were implemented on 4.73mm^2.

The power supply voltage was 3.3V and the power consumption was 46mW.

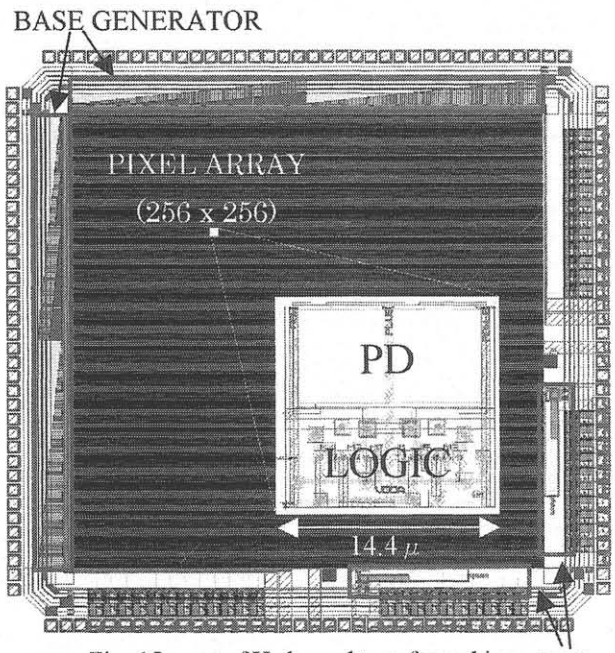

Fig. 4 Layout of Hadamard transform chip

4. Conclusions

The 256x256-pixel image sensor with the Hadamard transform function was designed with 0.35μm CMOS technology.

Acknowledgments

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References

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