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Implementation of OFDM Modem Using Radix-N Pipeline FFT Processor

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1. Introduction

Recently, the OFDM (Orthogonal Frequency Division Multiplexing) technique has been used widely in the mobile communication system. WLAN (Wireless Local Area Network) such as IEEE 802.11a LAN[1] can be a typical example of OFDM applications. In the implementation OFDM modem, FFT(Fast Fourier Transform) processor is a key component for modulation and demodulation parts. In the previous work[3], several kinds of pipeline structure of FFT are introduced. However, they (i.e., R2MDC, R2SDF, R4MDC, R4SDF, R4SDC) have the initial (2N-1)clock latency including bit-reverse block latency at least. Thus, these schemes are not appropriate to high-speed wireless LAN applications. In this paper, we propose a new FFT scheme with (2N-4) clock latency, and it's shorter clock latency enable the implementation of efficient wireless LAN modem.

2. Design of FFT processor

Radix-N decomposition

$$\begin{bmatrix} X(0)\\ X(1)\\ X(2)\\ X(3)\\ X(4)\\ X(5)\\ X(6)\\ X(7) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1\\ 1 & W_8^1 & W_8^2 & W_8^3 & W_8^4 & W_8^5 & W_8^6 & W_8^7\\ 1 & W_8^2 & W_8^4 & W_8^6 & W_8^8 & W_8^{10} & W_8^{12} & W_8^{14}\\ 1 & W_8^3 & W_8^6 & W_8^9 & W_8^{12} & W_8^{15} & W_8^{18} & W_8^{21}\\ 1 & W_8^4 & W_8^8 & W_8^{12} & W_8^{16} & W_8^{20} & W_8^{24} & W_8^{28}\\ 1 & W_8^5 & W_8^{10} & W_8^{15} & W_8^{20} & W_8^{25} & W_8^{30} & W_8^{35}\\ 1 & W_8^6 & W_8^{12} & W_8^{18} & W_8^{24} & W_8^{30} & W_8^{36} & W_8^{42}\\ 1 & W_8^7 & W_8^{14} & W_8^{21} & W_8^{28} & W_8^{35} & W_8^{42} & W_8^{49} \end{bmatrix} \times \begin{bmatrix} x(0)\\ x(1)\\ x(2)\\ x(3)\\ x(4)\\ x(5)\\ x(6)\\ x(7) \end{bmatrix} \quad (1)$$

where $W_N = e^{-j2\pi/N}$.

Eq.(1) shows the computation example of 8-point DFT-matrix. Eq.(1) can be significantly simplified by using eq.(2) and eq.(3).

$$W_N^{k+N/2} = -W_N^k \quad (2)$$

$$W_N^{k+N} = W_N^k \quad (3)$$

By using eq.(2) and eq.(3), eq.(1) can be decomposed two 4-point DFTs matrices of eq.(4) consisted of even and odd indexed term.

$$\begin{bmatrix} X(0)\\ X(1)\\ X(2)\\ X(3)\\ X(4)\\ X(5)\\ X(6)\\ X(7) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0\\ 1 & 0 & -j & 0 & -1 & 0 & j & 0\\ 1 & 0 & -1 & 0 & 1 & 0 & -1 & 0\\ 1 & 0 & j & 0 & -1 & 0 & -j & 0\\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0\\ 1 & 0 & -j & 0 & -1 & 0 & j & 0\\ 1 & 0 & -1 & 0 & 1 & 0 & -1 & 0\\ 1 & 0 & j & 0 & -1 & 0 & -j & 0 \end{bmatrix} \begin{bmatrix} x(0)\\ x(1)\\ x(2)\\ x(3)\\ x(4)\\ x(5)\\ x(6)\\ x(7) \end{bmatrix} + \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1\\ 0 & W_8^1 & 0 & -jW_8^1 & 0 & -W_8^1 & 0 & jW_8^1\\ 0 & -j & 0 & j & 0 & -j & 0 & j\\ 0 & -jW_8^1 & 0 & W_8^1 & 0 & jW_8^1 & 0 & -W_8^1\\ 0 & -1 & 0 & -1 & 0 & -1 & 0 & -1\\ 0 & -W_8^1 & 0 & jW_8^1 & 0 & W_8^1 & 0 & -jW_8^1\\ 0 & j & 0 & -j & 0 & j & 0 & -j\\ 0 & jW_8^1 & 0 & -W_8^1 & 0 & -jW_8^1 & 0 & W_8^1 \end{bmatrix} \begin{bmatrix} x(0)\\ x(1)\\ x(2)\\ x(3)\\ x(4)\\ x(5)\\ x(6)\\ x(7) \end{bmatrix} \quad \text{.....(4)}$$

Design of Radix-N pipeline FFT structure

Eq.(4) can be relocated by each two 4-point DFTs as shown in eq.(5). In this case of eq.(5), we can get the same results of 8-point DFT by executing 4-point DFT two times.

$$[X(0)\ X(1)\ X(2)\ X(3)\ X(4)\ X(5)\ X(6)\ X(7)]$$
$$= \begin{bmatrix} 1 & 1 & 1 & 1\\ 1 & -j & -1 & j\\ 1 & -1 & 1 & -1\\ 1 & j & -1 & -j \end{bmatrix} \times \begin{bmatrix} X(0)\\ X(2)\\ X(4)\\ X(6) \end{bmatrix} \pm \begin{bmatrix} 1 & 1 & 1 & 1\\ 1 & -j & -1 & j\\ 1 & -1 & 1 & -1\\ 1 & j & -1 & -j \end{bmatrix} \times \begin{bmatrix} X(1)\\ W_8^1 X(3)\\ -jX(5)\\ -jW_8^1 X(7) \end{bmatrix} \quad \text{..... (5)}$$

where twiddle factor W_N is only N/4 used.

By using decomposed method as shown in Eq.(5), we can made a Radix-N structure of N-point DFT as shown in Eq.(6). Fig.1 show the case of Radix-64 pipeline FFT structure for IEEE 802.11a wireless LAN.

$$\begin{aligned} &[X(0)\ X(1)\ \cdots\ X(63)] = \\ &= (\{\{R4[16n] \pm R4[16n+8\cdot W_8]\} \pm \{R4[16n+4] \pm R4[16n+12\cdot W_8]\}\cdot W_{16} \\ &\pm (\{\{R4[16n+2] \pm R4[16n+10\cdot W_8]\} \pm \{R4[16n+6] \pm R4[16n+14\cdot W_8]\}\cdot W_{16})\cdot W_{32} \\ &\pm (((\{\{R4[16n+1] \pm R4[16n+9\cdot W_8]\} \pm \{R4[16n+5] \pm R4[16n+13\cdot W_8]\}\cdot W_{16} \\ &\pm (\{\{R4[16n+3] \pm R4[16n+11\cdot W_8]\} \pm \{R4[16n+7] \pm R4[16n+15\cdot W_8]\}\cdot W_{16})\cdot W_{32})\cdot W_{64} \end{aligned}$$
$$\text{.....(6)}$$

where n= 0,1..3, R4[.] is Radix-4 BF PE , W_N is twiddle factor by N/4 numbers.

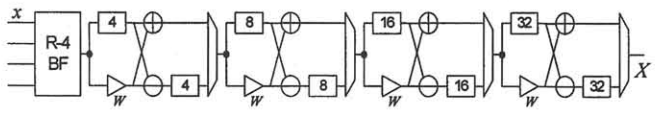

Fig 1. Radix-N pipeline FFT structure

Newly proposed pipeline structure has the three merits, first, CSD(Canonical Signed Digit) constant multipliers [5] are used for its complex multipliers. Because twiddle

factors are used N/4 only in their stages, So, We can improve hardware efficiency about 50% in respect of multiplications. And, second is its initial latency has 2N-4 clocks (including N clocks of bit-reverse unit). In IEEE802.11a wireless LAN specification , the MAC and PHY require to respond within 16μs with first symbol on the air interface of the earliest possible response frame. That is 4 OFDM symbol periods, commonly RF analog interface and MAC will take the period of one symbol, and de-interleaving process also takes one symbol period in receiver. So, FFT processing has to be processed in 2 symbol periods. Other kinds of pipeline structure of FFT (ie, R2MDC, R2SDF, R4MDC, R4SDF, R4SDC [3]) have the initial 2N-1 clock latency including bit-reverse block latency at least. So, these schemes are not appropriate to wireless LAN applications. Finally, it is easy to design because the control of two input MUX is not complex but simple.

3. Implementation of Radix-N pipeline IFFT/FFT structure in the WLAN Test-bed.

We implemented Test-bed of IEEE 802.11a WLAN as shown in the Fig.2. OFDM symbols are mixed with preamble short, long sequence, which is used for symbol synchronization. The Characteristics of each components of Implemented Test-bed are presented in the Table I. The key processor of implemented Test-bed is a Radix-N pipeline IFFT/FFT processor. They could process a data-rate of 20Mbps (T_{FFT}=3.2μs). Initial latency is (2N-4) clocks. This (2N-4) clocks are shorter than conventional initial (2N-1) clocks [3], this property enable the implementation of more efficient high-speed WLAN modem. The external data word length for both input and output is adopted to W=8bits real and imaginary part, individually. Fig 3 shows the measured OFDM symbols modulated by designed IFFT processor, demodulated signal by designed FFT processor. We can certify the efficient operation of IFFT/FFT processor in the Test-bed of IEEE 802.11a WLAN system.

4. Conclusions

In this paper, we propose a new Radix-N FFT processor with (2N-4) clock latency to implement IEEE 802.11a WLAN modem. The proposed scheme is not only easy to be designed, but also can be reduced hardware requirement by using the CSD constant multipliers instead of parallel complex multiplier. Furthermore, the efficient operation of IFFT/FFT processor are measured and certified using the implemented Test-bed of IEEE 802.11a WLAN system.

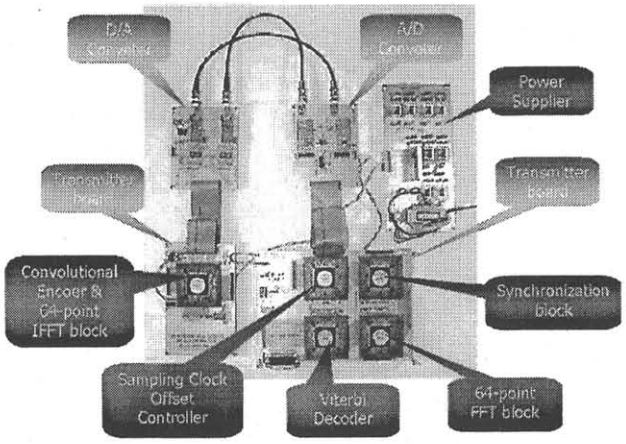

Fig 2. Implemented Test-bed of WLAN

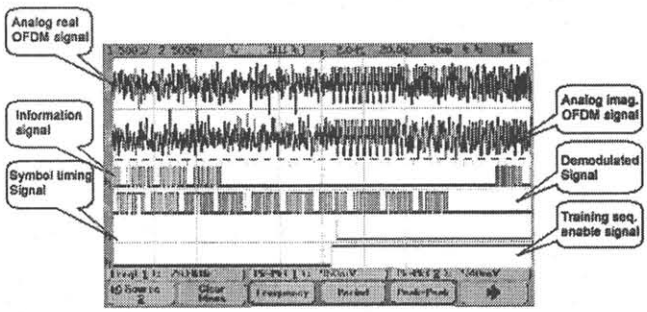

Fig 3. Measured OFDM signal using designed IFFT/ FFT processor

Table I. Characteristics of Implemented Test-bed of WLAN

Component	Characteristics
IFFT/FFT Processor	-Processing speed: 20Mbps -Initial latency: 124 clock times -Input /output bits: complex 8bits -(De) modulation method: 64QAM
Convolutional encoder	-Code rate of ½ -Constraint length of 7
Viterb decoder	-Register exchange method -Majority voting is available
Synchronizer	-Sync from Short, Long sequence -Signal detection, -Symbol synchronization
D/A, A/D	-ADC(AD9283), DAC(AD9708) -Bit resolution: complex 8 bit. -Output coding: offset binary code.

References

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