

P1-7

Switched Current Analog Programmable FIR filter for Software Defined Radio

Shigehito Saigusa, Seong-Kweon Kim, Hiroyuki Nakase, Suguru Kameda and Kazuo Tsubouchi

Research Institute of Electrical Communication, Tohoku University

Katahira 2-1-1, Aoba-ku, Sendai 980-8577, Japan

Phone: +81-22-217-5532 Fax: +81-22-217-5533 E-mail: shigusa@riec.tohoku.ac.jp

1. Introduction

Software defined radio (SDR) is a promising solution for multi-mode and multi-band mobile communication system [1]. One of key component of SDR is programmable filter, *i.e.*, the radio frequency/immediate frequency band pass filter, the root roll off filter and so on. Although the recent digital signal processing (DSP) operates at high frequency, power of consumption of the filters using DSP is over 100mW.

We have already proposed and implemented the current-cut switched current matched filter (CC-SIMF). The power consumption of CC-SIMF can be remarkably reduced [2].

In this paper, we propose the switched current analog programmable finite impulse response (FIR) filter for SDR terminals. New programmable tap circuits are proposed. Furthermore, implementation and measurement of the tap circuit are described and power consumption of 16-tap FIR filter is estimated.

2. New design method of the programmable FIR filter

Figure 1 shows the block diagram of the FIR filter. Since the current memory cells (CM) in the FIR filter are arrayed in parallel, no current transfer error accumulation occurs [3],[4]. According to the sampling clock pulse, the input current is transferred to and stored at one of CMs through the sampling switches, *i.e.*, one of the gates is activated at a certain sampling timing by the digital logic circuits. The tap circuit and the switched matrix determine the tap coefficient. The tap coefficient is cycled by the switched control logic.

The CM is shown in Fig.2. The CM is constructed with the current source, memory MOS, switches and the dummy MOS. The dummy MOS cancels the clock-feed-through error and the memory current accuracy of the CM increases [3].

The conventional tap circuit of the FIR filter is usually constructed with the gate width ratioed current mirror. However, the tap circuit has no programmability. A proposed tap circuit is shown in Fig.3. The circuit is constructed with the current mirrors and switches. When the SW_x is on, the current flow into *i*_{out} line, where *x* = 1,...,5. The current flow through the SW₁ is half of, SW₂ is fourth part of, the SW₃ is eighth part of and the SW₄ and the SW₅ is sixteenth part of the input current. In Fig.3, the rounding step of the tap circuit is 0.0625. Figure 4 shows the bit error rate (BER) characteristics of root roll

off filter as a function of the individual rounding step with computer simulation. The tap number is 16. The over sampling rate is 4. As shown in Fig.4, degradation of the BER characteristic of 0.0625-step rounding coefficient is negligible to be compared with that of non-step rounding coefficient.

The power consumption of the FIR filter using this tap circuit is summarized in Table I. The estimated power consumption of 0.2μm 16-tap current-cut FIR filter is 3.0mW.

3. Fabrication and evaluation

We have fabricated 0.0625-step rounding tap circuit using 0.35μm CMOS mixed signal technology. The foundry is AMS (Austria Mikro Systeme). The broker is CMP (Circuit Multi-Projets, France). Figure 5 shows the fabricated 0.0625-step rounding tap circuit. Size of the tap circuit is 210μm x 140μm.

Figure 6(a) shows the simulated and measured waveform at 100kHz with clock timing pulse of switches in Fig. 6(b). The input current is 10μA. The maximum error between measured and simulated current is 13%. For the implementation of this work, we have not optimized the layout of the tap circuit. Suitable layout of the tap circuit enables this error to be small. The measured maximum operation frequency is 4MHz. This is because the maximum operation frequency is limited by the conversion speed of the off-chip V-I/I-V converter circuit using the operational-amplifier. The settling time of the tap circuit with the SPICE simulation is less than 5ns. With the on-chip V-I/I-V converter, this circuit can operate at higher frequency.

4. Conclusion

We have proposed the switched current analog programmable finite impulse response (FIR) filter. A proposed new tap circuit has programmability. The FIR filter is promising solution for analog programmable filter in software defined radio system.

References

- [1] J. Mitola, IEEE Communication Magazine, vol.33 No.5, (1995) p. 26.
- [2] K. Tsubouchi and K. Masu, *Proc. of Int. Symp. of Future of Intellectual Integrated Electronics* (1999) p.259
- [3] K. Togura, K. Kubota, K. Masu and K. Tsubouchi, *Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, 1999* (1999) p. 442.

[4] K. Togura, H. Nakase, K. Kubota, K. Masu and K. Tsubouchi, IEICE Trans. Electron., vol.E84-C. no.2. 212 (2001)

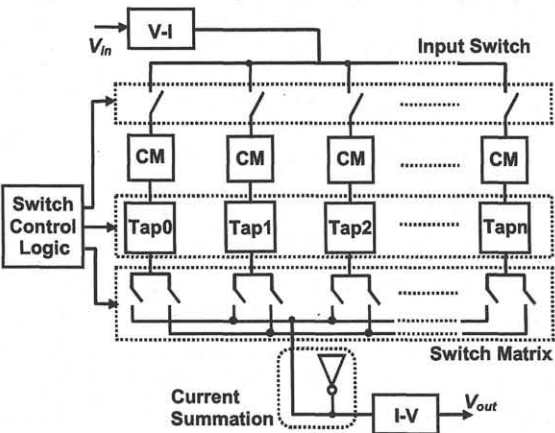


Fig. 1 Circuit block diagram of FIR filter.

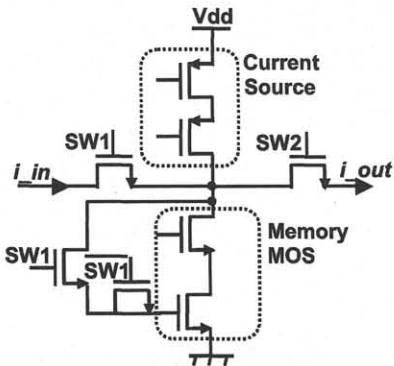


Fig. 2 Current memory cell.

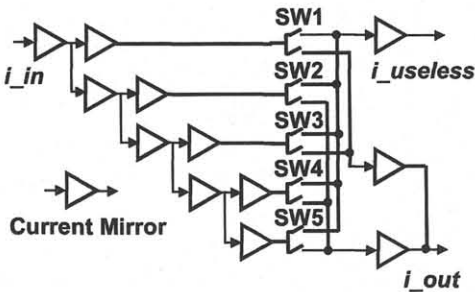


Fig. 3 0.0625-step rounding tap circuit.

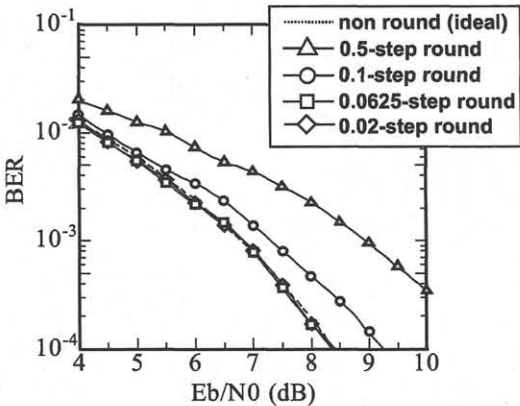


Fig.4 BER estimated by rounding step.

Table. I Power consumption (estimation)

Bias current of each cell	100μA
Current source of each cell	1
Number of cell	16
Bias current of summation circuit	400μA
Number of current source of tap circuit	24
Number of current source of summation circuit	4
Total static current without current cut	38.9mA
Consumed power with current cut ¹⁾	3.0mW

1) 90% Current cut estimated with 16-tap using 0.2μm CMOS technology

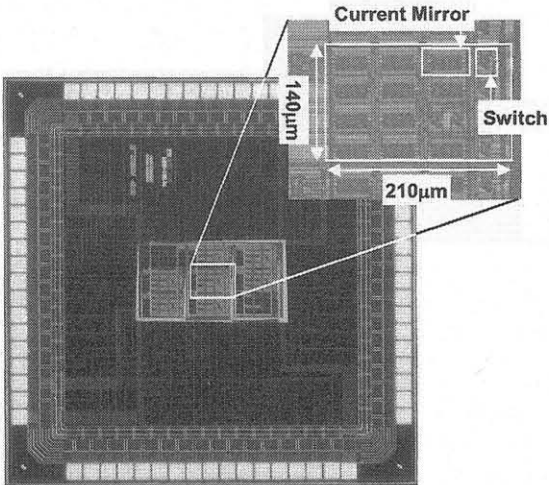


Fig. 5 0.0625-step rounding tap chip using 0.35μm CMOS technology.

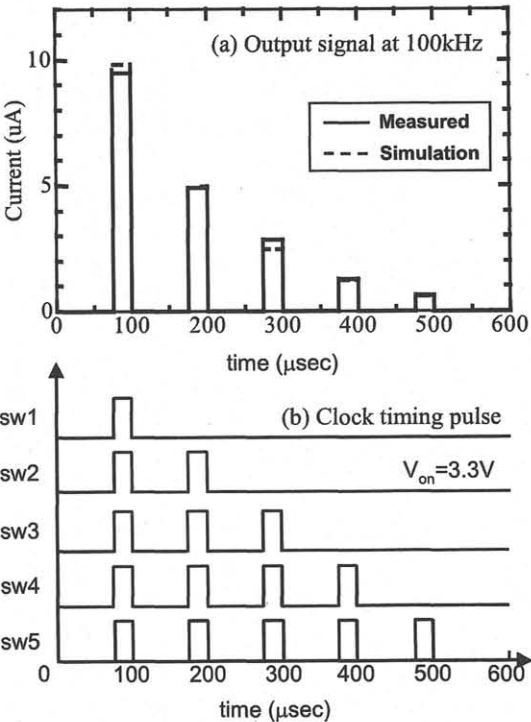


Fig. 6 (a) Output signal at 100kHz of the fabricated 0.0625-step rounding tap and (b) clock timing pulse of switches.