P10-2

A Novel Soft-program Scheme for More than 2-bits Multi-level Cell Flash Design

T.H. Fan, C.C. Yeh, T.C. Lu, and Sam Pan

Macronix International Co. Ltd.,
No. 16, Li-Hsin Road, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.
Tel: 886-2-5786688 EXT: 78033; Fax: 886-2-5789087; E-mail: thfan@mxic.com.tw

1. Abstract

Threshold voltage placement is critical for multi-level cell (MLC) flash design. However, most published 2-bits MLC designs focus on programming controllability. In this work, a novel soft-program scheme is proposed to tighten the threshold voltage distribution in first level, reduce cycling induced read disturb, and avoid programming inaccuracy. This technique is essential for more than 2-bits MLC flash design.

2. Introduction

In conventional one bit per cell flash memories, information is stored in two Vth levels corresponding to "1" or "0" states. For MLC flash memories, it is possible to store information in more than 2 levels. Three key issues to achieve MLC operation are precise Vth placement, accurate current sensing, and excellent charge retention. So far, it is reported that in addition to a tight Vth distribution, the spreading of the Vth distribution after bake, and cycling degradation is very critical for MLC device consideration [1-3]. However, the large Vth distribution after erase in 1st level and read disturb could be the bottleneck for more than 2-bits MLC flash design. A lot of converge and soft-program methods have been proposed to overcome this issue [4]. Unfortunately, the 1st level Vth distribution is still too large and the cells in main distribution is not electrical annealed. In this paper, we will demonstrate the smart soft-program technique can significantly improve MLC flash design margin and achieve more than 2-bits MLC flash memories.

3. Analysis and Results

In addition to geometry induced fast erase, abnormal fast erase due to positively charge centers during cycling has been reported [5]. To remedy the fast erase behavior, soft-program is essential to bring up the low Vth of fast erased bits. In conventional soft-program scheme, as depicted in Fig.1a, most soft-program current flows into the over-erased cell (cell B in Fig.1a) because of its ultra low erased Vth, while the cells in main distribution are not electrical annealed (such that cell A in Fig.1a). By this way, the Vth distribution in 1st level, as shown in Fig.2, can only be converged to around 2V. Besides, the read disturb of cells in main distribution are significant. Both these factors reduce the MLC design margin. In the following, as depicted in Fig.1b, a smart soft-program scheme is proposed. It erases the fresh cells to a lower erase-verify voltage (EV1), then a stepping gate voltage and a constant drain voltage are applied to the memory cell, which is similar to conventional MLC program method [6], followed by bit-by-bit verify to a higher erase-verify voltage (EV2). Thus not only the over-erased cell but also the cell with higher Vth can be soft-programmed (cell C and cell D in Fig.1b). Consequently, the Vth distribution in the 1st level can be reduced to 1V by using this smart soft-program scheme as shown in Fig.3. As compared to the conventional one, more than 1V design margin can be obtained using this new scheme.

In addition to tighten the Vth distribution in 1st level, the read disturb on the selected cell is also improved. The selected word-line places the control gate of the erased cells at, for example, 6.0V. The selected cell's drain is biased at about 1.2V. Fig.4 shows the read disturb characteristics of 100 &100K P/E cycled cell with conventional soft-program scheme, which cell dimension is W/L=0.3/0.3um. The read disturb characteristics of cell B (with Vth brought up by soft-program, as shown in Fig.1) shows a linear time dependent in both 100 & 100K cycling cases. On the other hand, cell A (no Vth shift after soft-program) shows an abrupt increase in Vth shift around 10^3 seconds in both 100 & 100K cycling cases. It indicates that the read disturb become worse if no soft-program is applied to the P/E cycled cells. Since the captured charges are not annihilated by soft-program (cell A) during read disturb, the abnormal Vth shifts in the erased memory cell can cause a reduction of Vth margin, which must be carefully considered for MLC flash design because the threshold voltage intervals in MLC flash are much narrower than conventional flash memory.

In comparison, the read disturbs characteristics of 100 & 100K P/E cycled cells with smart soft-program scheme are shown in Fig.5. Cell C and D are both soft-programmed due to the stepping gate voltage in the smart soft-program scheme. Intently, no abrupt Vth shift increase is observed. It is believed that induced damages in both cells can be annihilated by electron injection during smart soft-program.

The charge pumping (CP) experiment is done by fixed based level voltage (V_b) and varying high-level gate voltage (V_{gh}). As shown in Fig.6, charge pumping current (I_{CP}) increases after fixed P/E cycles indicating that positive trapped charges and interface states are generated. I_{CP} versus V_{gh} on 100 and 10K cycled cells with or without smart soft-program are plotted in Fig.7. It is clearly demonstrated that the positive trapped charges are dramatically annihilated by the smart soft-program in both 100 & 100K cycling cases since I_{CP} curve shifting indicate positive charge annihilation. We believed that the positive trapped charges can be neutralized by the injected carriers during smart soft-program instead of trapped charges de-trapping because no annihilation was seen if the soft-program in done by gate voltage pulse stress only (Vcg=5V).

Precise Vth placement is also very important in MLC flash due to its narrow design margin. Not only the erased Vth increases significantly if the positive trapped charges is present, but also the abnormal program behavior will occur during channel hot electron (CHE) program. Fig.8 shows the program characteristics of these two schemes, which gate and drain voltage is constant in CHE program. As shown in Fig.8, fast program will occur in cell A (without soft-program in conventional scheme) after 100K cycling. However, the fast program behavior disappears when the positively trapped charges are annihilated by the smart soft-program scheme mentioned above (cell C).

4. Conclusions

With the smart soft-program method, the 1st level Vth distribution can be reduced, the Vth rise during read disturb in the 1st Vth level can be minimized, and over-program issues in 2nd and 3rd programmed states can be avoided. These improvements are essential for more than 2-bits MLC flash memories design, as shown in Fig.9.
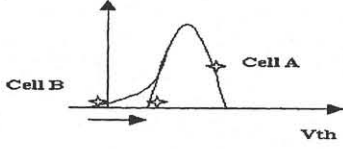
Acknowledgments

References

[1] H. Shiga et al, *Symp. VLSI Circs.*, pp.33,1999.
[2] A. Nozoe et al, *IEEE, ISSCC*, pp.110, 1999.
[3] P. Candelier et al, *IEEE, IRPS*, pp.104, 1997.

[4] S. Yamada et al, *IEEE, TED,* Vol.43, No.11, pp.1937, 1996.
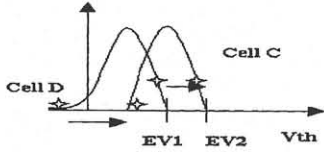[5] A. Brand et al, *IEEE, IRPS*, pp.127, 1993.
[6] G. J. Hemink et al, *Symp. VLSI Tech.*, pp.129, 1995.

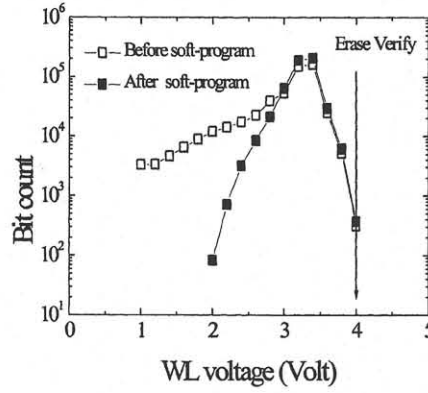Fig.1 The conventional and proposed smart soft-program schemes. Cell A, cell B, cell C, and cell D are shown.

Fig.2 Vth distribution after soft-program in the conventional soft-program scheme.
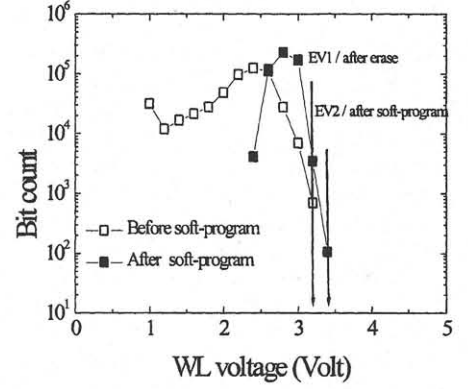
Fig.3 Vth distribution after soft-program in the smart soft-program scheme.
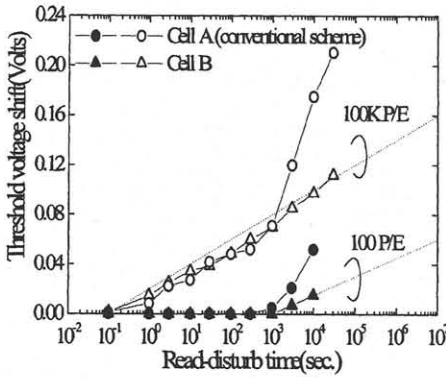
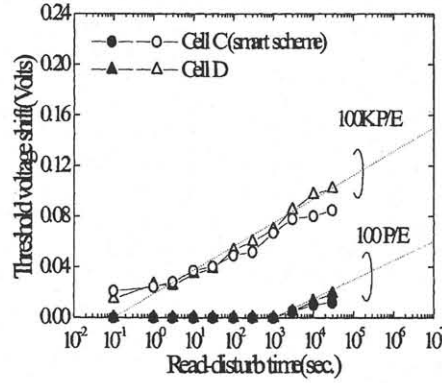Fig.4 Read Disturb of cell A and cell B in the conventional soft-program scheme.

Fig.5 Read Disturb of cell C and cell D in the smart soft-program scheme.
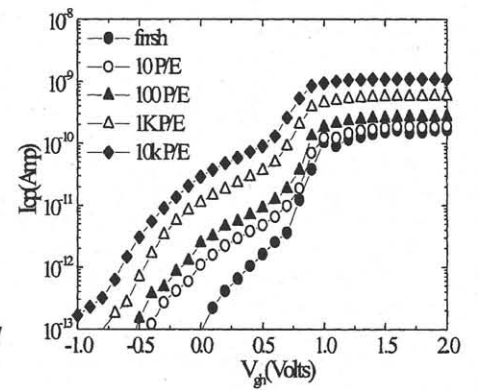

Fig.6 I_{CP} versus V_{gh} after various P/E cycles. More positive trapped charges and interface states are generated.
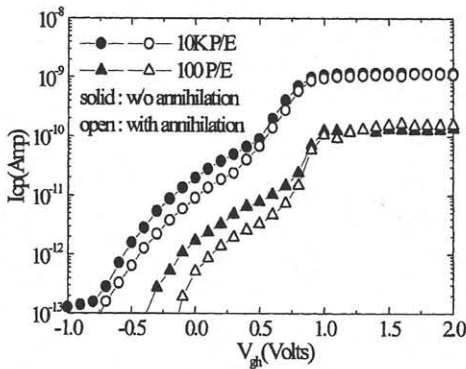

Fig.7 I_{CP} versus V_{gh} after P/E cycling. I_{CP} is shifted by smart soft-program due to positive charge annihilation.
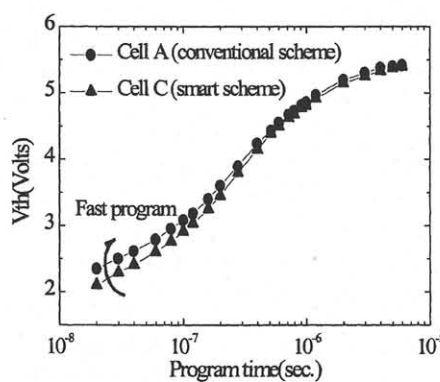

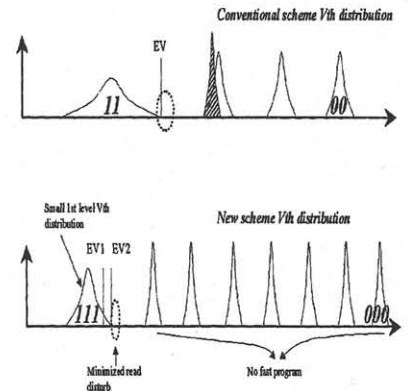Fig.8 Program performance of cell A and C using constant gate and drain voltages.

Fig.9 More MLC levels can be obtained using the smart soft-program scheme.