Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 612-613

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AHE: A New Low Voltage /High Speed Programming Scheme for Both N- and P-Channel Flash EEPROM's

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Abstract- Two strategies are commonly used to design high performance ETOX flash cells. One is based on the cell structure approach such as p-channel[1] or p-floating gate[2], and the other one is using different operation schemes. In the design of low voltage or low power flash cells, several programming schemes have been of interests, such as CHISEL[3], DAHE(Drain Avalanche Hot Electron) [4], and SCIHE[5] etc. For the first time, we report a new programming scheme which is well suited for both n- and p-channel flash cells. This programming is achieved by substrate bias enhanced Avalanche Hot-Electron (AHE) injection. In particular, it allows programming at very low terminal voltages within +5V and -5V. In terms of the performance, the present scheme is faster than CHE or BBHE [6] scheme. In terms of the reliabilities, better gate- and drain-disturb, reasonable endurance, can be achieved for both n- and p-channel cells owing to a low voltage operation. Also, for the retention characteristics, AHE scheme shows much better benefit for n-channel cells.

Device Preparation and Measurements

The cell structure used in this study is a conventional stacked-gate(ETOX) flash memory cell fabricated by 0.35μm triple well technology both for the n-channel and p-channel cells. The thickness of tunnel oxide/effective ONO interpoly dielectric are 100Å/210Å and 90Å/165Å for n-channel and p-channel cells respectively. Fig. 1 shows the schematic diagram of the new AHE scheme along with the operating conditions. Note that the terminal voltages are kept within +5V and -5V for programming in the new scheme.

Results and Discussion

A. The Scheme and Cell Performance

The mechanism of the new scheme is as follows. First, the drain/substrate junction is biased in the avalanche region, from which electrons and holes are generated. Then, the hot electrons will surmount the barrier and contribute to the gate current via an appropriate field between the gate and the substrate or the drain. Fig. 2 shows the gate and drain current of n-cells. The injection efficiency defined as I_G/I_D is about 10^{-5}~10^{-6} for both type of cells using AHE scheme. It is larger than that of the conventional CHE and less than that of the BBHE[6]. The programming characteristics of AHE for n- and p-channel cells are shown in Figs. 3 and 4, respectively. AHE scheme is always faster than CHE scheme in n-cell and BBHE in p-cell. In extreme case, the programming speed as fast as nano-second range can be achieved. The convergence speed of n-channel cell using AHE scheme is faster than that of normal CHE scheme.

B. Cell Reliabilities

Disturb Characteristics: For the evaluation of disturb, the gate and drain disturb will be taken into consideration. Fig. 5 shows the results of gate disturb for the new AHE scheme and their comparison with conventional scheme in both n- and p-channel cells respectively. The gate disturb is nearly eliminated in the present scheme since much lower control gate voltage is used in the new scheme. This is one of the major benefit. Through the help of a substrate bias, drain disturb can also be greatly reduced for p-channel cells as given in Fig. 6, in which a 3-order improvement of the drain disturb can be achieved. However, the drain disturb is almost the same by using either the present scheme or CHE scheme.

Data Retention Characteristics: The experimental data retention characteristics are shown in Fig. 7. This figure shows the threshold voltage shift of the cells before and after P/E cycles baked at 250°C. It is obvious that AHE has a much better data retention by comparing with that of CHE. However, no advantage for the p-cell based on the AHE scheme. But, this can be remedied by a device drain engineering.

Endurance: The reliability of the flash cell with AHE both for n- and p-channel cells has also been examined for the endurance characteristics. The CHE for n-channel cells and BBHE for p-channel cells are used as a reference. All of the experimental cells use channel Fowler-Nordheim(FN) for erase. Fig. 8 shows the endurance characteristics for n-channel cells. After the cycling, similar results of the window closure are observed for n-cell. However, for the p-cells, the window closure is relaxed for both AHE and BBHE schemes. (P-channel cell endurance will be shown during the presentation).

Comparison with Reported Schemes: The present scheme shows slight difference with reported schemes but exhibits uunique features. For a comparison, please see the GIDL measurement in Fig. 9. The present AHE scheme is faster and reliable than the CHISEL[3] scheme since more electron sources are generated in the drain which gives large gate current injection. SCIHE[5] is a combination of CHISEL and DAHE[4], which gives a poorer reliability by comparing with the present AHE scheme. Although the DAHE scheme has better reliability, it has disadvantages with a high voltage and lower speed. In short, a low voltage operation should be achieved by a substrate bias and with suitable sources of electrons for injection purpose.

In summary, we demonstrated a new programming scheme, substrate-bias enhanced AHE, for both n- and p-channel flash cells. It is achieved by a combination of the avalanche hot electron injection in the drain and an applied substrate bias. This scheme features low voltage and high speed operation. Results show that the present scheme exhibits many advantages for applications to n- or p-channel cell. These include a faster programming speed, low voltage,low power, faster convergence, better gate disturb, and drain disturb characteristics. Moreover, in extreme case, a record high speed with 20 nsec programming for a state-of-the-art ETOX flash cell technology can be achieved. Also, it is well suited for low voltage and high reliability applications.

Acknowledgments This work was sponsored by the NSC, Taiwan, under contract No. NSC89- 2218-E009-110.

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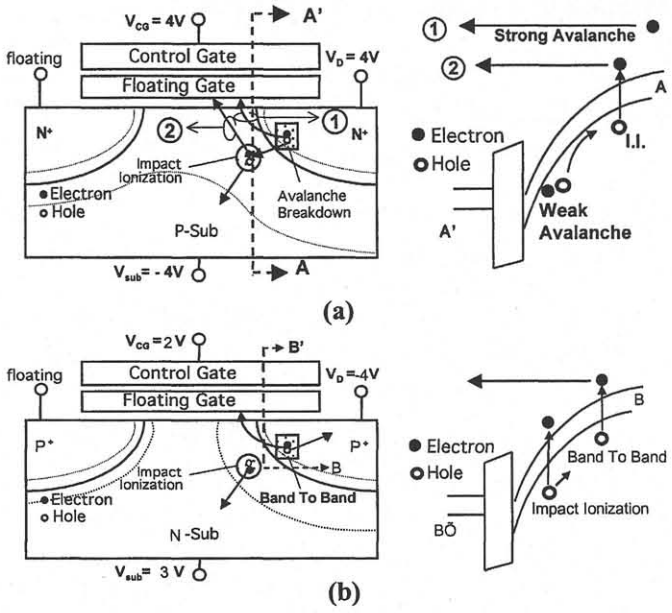

Fig. 1 Schematic diagram of the new programming scheme for (a) n-channel, and (b) p-channel flash cells.

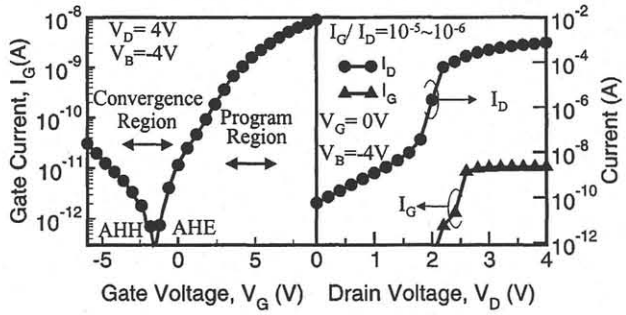

Fig. 2 The gate and drain current characteristics for n-channel cells. The operating bias for better injection efficiency in AHE scheme is $V_D > 2.5V$.

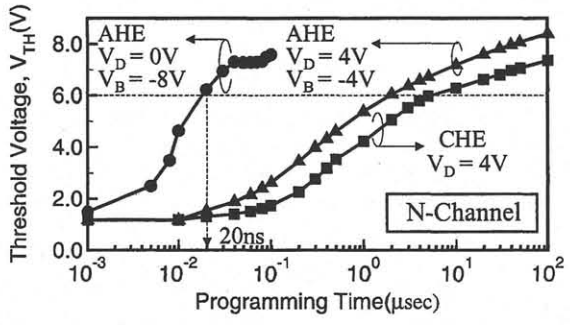

Fig. 3 Programming characteristics for AHE and CHE schemes in n-channel cell. Note that a 20nsec speed can be achieved with V_B= -8V.

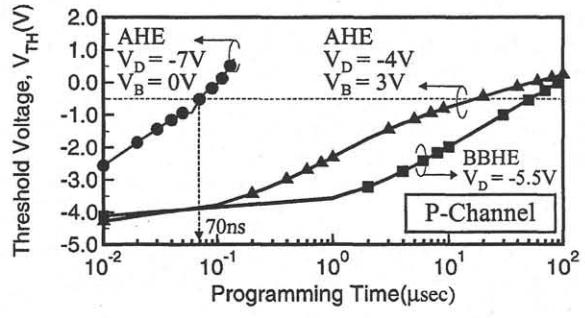

Fig. 4 Programming characteristics for AHE and BBHE schemes in p-channel cell. Note that a 70nsec speed can be achieved with V_D=-7V.

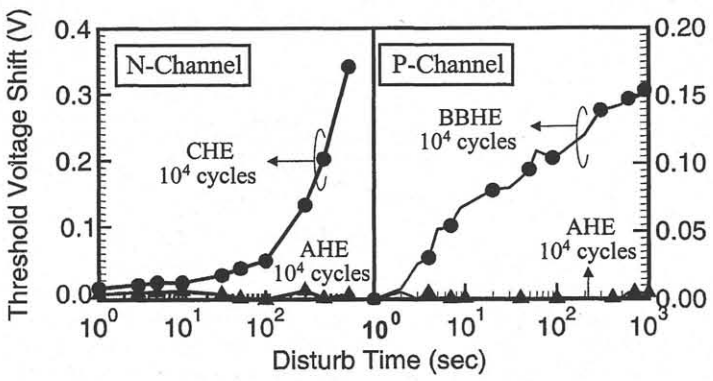

Fig. 5 The gate-disturb characteristics for (left) both AHE and CHE in n-channel and (right) both AHE and BBHE in p-channel flash cells. Note that a much lower gate disturb is observed for new scheme as a result of a lower gate voltage for programming.

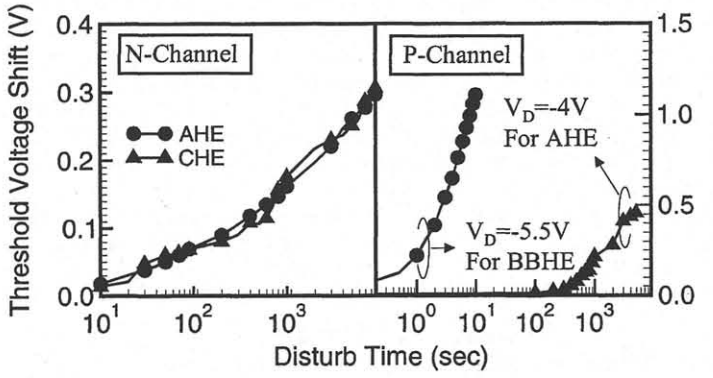

Fig. 6 The drain-disturb characteristics for (left) both AHE and CHE in n-channel and (right) both AHE and BBHE in p-channel flash cells. Note that a dramatic improvement for p-channel cell can be achieved.

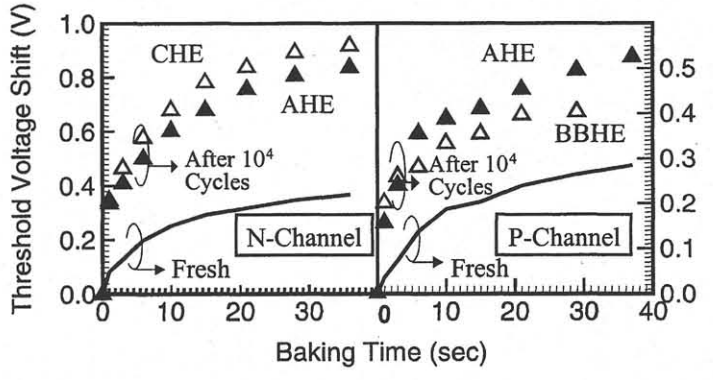

Fig. 7 The comparison of the data retention characteristics between AHE and CHE for n-channel cells, AHE/BBHE for p-channel cells after 10^4 long term P/E cycles.

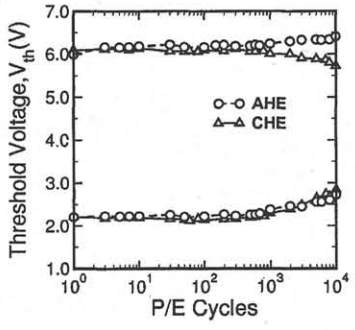

Fig. 8 Comparison of the endurance characteristics between AHE and CHE schemes for n-channel flash cells.

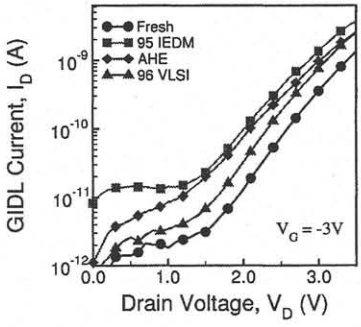

Fig. 9 Comparison of the P/E cycling induced GIDL currents between AHE and reported schemes for n-channel flash cells.